256Mb Synchronous DRAM Specification

A3V56S30GTP

A3V56S40GTP

Industrial Version

Zentel Electronics Corp.

General Description

A3V56S30GTP is organized as 4-bank x 8,388,608-word x 8-bit Synchronous DRAM with LVTTL interface and A3V56S40GTP is organized as 4-bank x 4,194,304-word x 16-bit. All inputs and outputs are referenced to the rising edge of CLK. A3V56S30GTP and A3V56S40GTP achieve very high speed data rates up to 166MHz, and are suitable for main memories or graphic memories in computer systems.

Features

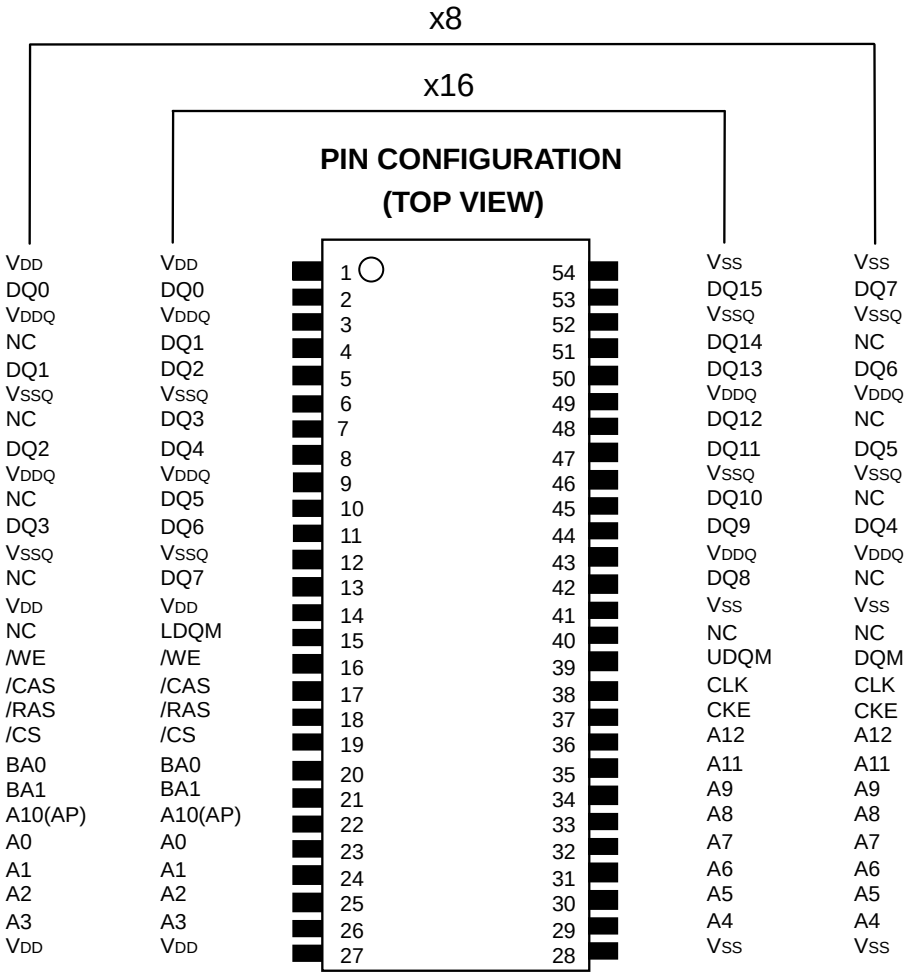
- Single 3.3V ±0.3V power supply
- Maximum clock frequency:
  -60:166MHz<3-3-3>/-70:143MHz<3-3-3>/-75:133MHz<3-3-3>
- Fully synchronous operation referenced to clock rising edge
- 4-bank operation controlled by BA0, BA1 (Bank Address)
- CAS latency- 2/3 (programmable)
- Burst length- 1/2/4/8/FP (programmable)
- Burst type- Sequential and interleave burst (programmable)
- Byte Control- DQM (A3V56S30GTP), LDQM and UDQM (A3V56S40GTP)
- Random column access
- Auto precharge / All bank precharge controlled by A10
- Support concurrent auto-precharge
- Auto and self refresh
- 8192 refresh cycles /64ms
- Temperature range: -40℃ to +85℃
- AEC-Q100 Grade3 compliant
- LVTTL Interface
- Package:
  400-mil, 54-pin Thin Small Outline (TSOP II) with 0.8mm lead pitch
  Pb-free package is available

Ordering Information

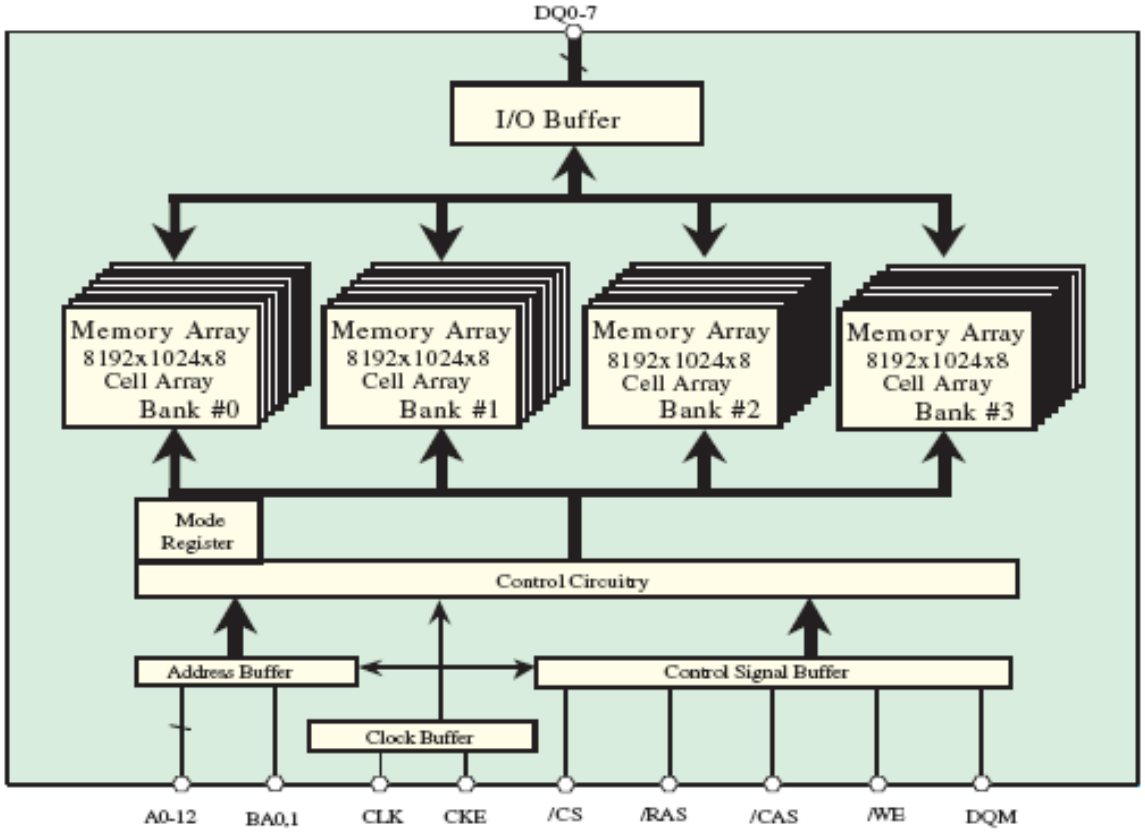
Part Number	Organization (words x bits)	Max. Frequency	CAS Latency	Supply Voltage
A3V56S30GTP-60I	32M x 8	166MHz	3	3.3V
A3V56S30GTP-70I		143MHz		
A3V56S30GTP-75I		133MHz		
A3V56S40GTP-60I	16M x 16	166MHz		
A3V56S40GTP-70I		143MHz		
A3V56S40GTP-75I		133MHz		

Zentel Electronics reserves the right to change products or specification without notice.

Pin Configuration (Top View)



CLK	: Master Clock	DQM	: Output Disable / Write Mask (A3V56S30GTP)
CKE	: Clock Enable	U,L DQM	: Output Disable / Write Mask (A3V56S40GTP)
/CS	: Chip Select	A0-12	: Address Input
/RAS	: Row Address Strobe	BA0,1	: Bank Address
/CAS	: Column Address Strobe	V_{DD}	: Power Supply
/WE	: Write Enable	V_{DDQ}	: Power Supply for Output
DQ0-7	: Data I/O (A3V56S30GTP)	V_{SS}	: Ground
DQ0-15	: Data I/O (A3V56S40GTP)	V_{SSQ}	: Ground for Output



Note: This figure shows the A3V56S30GTP
The A3V56S40GTP configuration is 8192x512x16 of cell array and DQ0-15

Type Designation Code

A 3 V 56 S 3 0G TP - 60 I

Option Code	I :Industrial temperature range (-40 ~ 85℃)
Speed	75: 133MHz@CL=3 70: 143MHz@CL=3 60: 166MHz@CL=3
Package Type	TP: TSOP II
Die Version	0G: Version 0G
I/O Configuration	3: x8 ; 4: x16
Classification	S: SDR
Density	56: 256Mb
Interface	V: LVTTL
Product Line	3: DRAM
Zentel Memory	

Pin Descriptions

SYMBOL	TYPE	DESCRIPTION
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank), or CLOCK SUSPEND operation (burst / access in progress). CKE is synchronous except after the device enters self refresh mode, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during self refresh mode, providing low standby power. CKE may be tied HIGH.
/CS	Input	Chip Select: /CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when /CS is registered HIGH. /CS provides for external bank selection on systems with multiple banks. /CS is considered part of the command code.
/CAS, /RAS, /WE	Input	Command Inputs: /CAS, /RAS, and /WE (along with /CS) define the command being entered.
DQM, LDQM, UDQM,	Input	Input / Output Mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output disable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when during a READ cycle. DQM corresponds to DQ0–DQ7 (A3V56S30GTP). LDQM corresponds to DQ0–DQ7, UDQM corresponds to DQ8–DQ15 (A3V56S40GTP).
BA0, BA1	Input	Bank Address Input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A0–A12	Input	A0-12 specify the Row / Column Address in conjunction with BA0,1. The Row Address is specified by A0-12. The Column Address is specified by A0-9(x8) and A0-8(x16). A10 is also used to indicate precharge option. When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, all banks are precharged.
DQ0–DQ15	I/O	Data Input / Output: Data bus.
NC	–	Internally Not Connected: These could be left unconnected, but it is recommended they be connected or V_{SS}.
V_{DDQ}	Supply	Data Output Power: Provide isolated power to output buffers for improved noise immunity.
V_{SSQ}	Supply	Data Output Ground: Provide isolated ground to output buffers for improved noise immunity.
V_{DD}	Supply	Power for the input buffers and core logic.
V_{SS}	Supply	Ground for the input buffers and core logic.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Operating ambient temperature	T_A	-40~ 85	°C
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

Notes:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operating Conditions (Recommended operating conditions, voltage referenced to V_{SS} = 0V, T_A = -40 to 85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
	V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	V_{DD}	V_{DD} + 0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -0.1mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 0.1mA
Input leakage current	I_{IL}	-10	-	10	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	3

Note:
1. V_{IH}(max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. V_{IL}(min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ V_{IN} ≤ V_{DD} + 0.3V, all other pins are not under test = 0V.
4. Dout is disabled , 0V ≤ V_{OUT} ≤ V_{DD}.

Capacitance (V_{DD} = V_{DDQ} = 3.3V, T_A = 25°C, f = 1MHz, pin under test biased at 1.4V.)

Parameter	Symbol	Min	Max	Unit	Note
Clock	C_{CLK}	2	3.5	pF	
/CAS,/RAS,/WE,/CS,CKE, U/L DQM	C_{IN}	2	3.5	pF	
Address	C_{ADD}	2	3.5	pF	
DQ0~DQ15	C_{OUT}	3.5	5.5	pF	

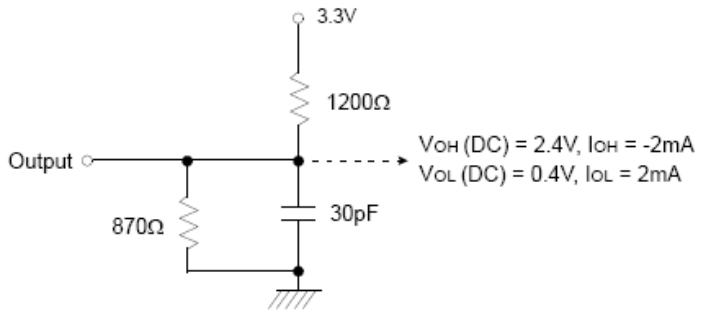
DC Characteristics (Recommended operating conditions unless otherwise noted, T_A =-40 to 85°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-60	-70	-75		
Operating Current (One Bank Active)	I_{CC1}	Burst length = 2 t_{RC} = t_{RC}(min) I_O = 0 mA	80	75	70	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE = V_{IL}(max), t_{CC} = 10ns	10				
	I_{CC2PS}	CKE & CLK = V_{IL}(max), t_{CC} = ∞	5				
Precharge Standby Current non power-down mode	I_{CC2N}	CKE = V_{IH}(min), CS = V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	30				
	I_{CC2NS}	CKE = V_{IH}(min), CLK = V_{IL}(max), t_{CC} = ∞ Input signals are stable	25				
Active Standby Current power-down mode (One Bank Active)	I_{CC3P}	CKE = V_{IL}(max), t_{CC} = 10ns	30				
	I_{CC3PS}	CKE & CLK = V_{IL}(max), t_{CC} = ∞	25				
Active Standby Current non power-down mode (One Bank Active)	I_{CC3N}	CKE = V_{IH}(min), CS = V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	50				
	I_{CC3NS}	CKE = V_{IH}(min), CLK = V_{IL}(max), t_{CC} = ∞ Input signals are stable	35				
Operating Current (Burst Mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs	100	90	85		1
Refresh Current	I_{CC5}	t_{ARFC} = t_{ARFC}(min)	115	100	95		2
Self Refresh Current	I_{CC6}	CKE = 0.2V	5	5	5		

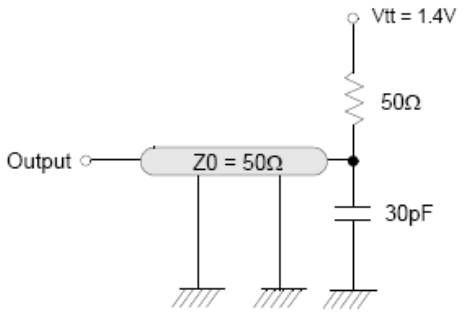
Notes:
1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(V_{IH} /V_{IL}=V_{DDQ}/V_{SSQ}).

AC Operating Test Conditions (V_{DD} = V_{DDQ} = 3.3V ±0.3V, T_A = -40 to 85°C)

Parameter	Value	Unit
AC input levels (V_{IH}/V_{IL})	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	Ns
Output timing measurement reference level	1.4	V
Output load condition	See Figure 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

Operating AC Parameter (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version			Unit	Note
		-60	-70	-75		
Row active to row active delay	tRRD(min)	12	14	15	ns	1
RAS to CAS delay	tRCD(min)	18	20	20	ns	1
Row precharge time	tRP(min)	18	20	20	ns	1
Row active time	tRAS(min)	42	45	45	ns	1
	tRAS(max)	100	100	100	us	
Row cycle time	tRC(min)	60	63	65	ns	1
Last data in to row precharge	tRDL(min)	2	2	2	CLK	2
Last data in to Active delay	tDAL(min)	5	5	5	CLK	
Last data in to new col. address delay	tCDL(min)	1	1	1	CLK	2
Last data in to burst stop	tBDL(min)	1	1	1	CLK	2
Mode register set cycle time	tMRD(min)	2	2	2	CLK	
Refresh interval time	tREF(max)	64	64	64	ms	
Auto refresh cycle time	tARFC(min)	60	70	75	ns	

Notes:

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.

AC Characteristics (AC operating conditions unless otherwise noted)

Parameter		Symbol	-60		-70		-75		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC (3)	6		7		7.5		ns	1
	CAS latency=2	tCC (2)	10		10		10			
CLK to valid output delay	CAS latency=3	tSAC (3)		5.4		5.4		5.4	ns	1,2
	CAS latency=2	tSAC (2)		5.4		5.4		6		
Output data hold time	CAS latency=3	tOH (3)	2.5		2.5		2.5		ns	2
	CAS latency=2	tOH (2)	2.5		2.5		2.5			
CLK high pulse width		tCH	2.5		2.5		2.5		ns	3
CLK low pulse width		tCL	2.5		2.5		2.5		ns	3
Input setup time		tSI	1.5		1.5		1.5		ns	3
Input hold time		tHI	1		1		1		ns	3
Transition time of CLK		tT	0.3	1.5	0.3	1.5	0.3	1.5	ns	
CLK to output in Low-Z		tSLZ	1		1		1			
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		5.4		5.4	ns	
	CAS latency=2			5.4		5.4		6		

Notes:
1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

Truth Table

Command Truth Table

COMMAND	Symbol	CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	BA1	BA0	A10/ AP	A12-11, A9 ~ A0
Device deselect	DSL	H	X	H	X	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X	X
Burst stop	BST	H	X	L	H	H	L	X	X	X	X
Read	RD	H	X	L	H	L	H	V	V	L	V
Read with auto precharge	RDA	H	X	L	H	L	H	V	V	H	V
Write	WR	H	X	L	H	L	L	V	V	L	V
Write with auto precharge	WRA	H	X	L	H	L	L	V	V	H	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	X	H	X
Mode register set	MRS	H	X	L	L	L	L	L	L	L	OP code

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

CKE Truth Table

Current state	Function	Symbol	CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	/Address
Activating	Enter Clock suspend or Active power down		H	L	L	V	V	V	V
			H	L	H	X	X	X	X
Clock suspend or Active power down	Maintain Clock suspend or Active power down		L	L	X	X	X	X	X
Clock suspend or Active power down	Exit Clock suspend or Active power down		L	H	X	X	X	X	X
All banks idle	Auto refresh command	REF	H	H	L	L	L	H	X
All banks idle	Enter Self refresh	SREF	H	L	L	L	L	H	X
All banks idle	Enter Precharge power down		H	L	L	H	H	H	X
			H	L	H	X	X	X	X
Self refresh	Exit Self refresh		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Precharge power down	Exit Prechage power down		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Precharge power down	Maintain Precharge power down		L	L	X	X	X	X	X

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Function Truth Table

Current state	/CS	/RAS	/CAS	/WE	/Address	Command	Action	Notes
Idle	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	ILLEGAL	2
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	2
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	2
	L	L	H	H	BA,RA	ACT	Bank active	
	L	L	H	L	BA,A10	PRE/PALL	NOP	4
	L	L	L	H	X	REF	Auto refresh	5
	L	L	L	L	OC	MRS	Mode register set	5
Row active	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	ILLEGAL	2
	L	H	L	H	BA,CA,A10	RD/RDA	Begin read, determine AP	
	L	H	L	L	BA,CA,A10	WR/WRA	Begin write, determine AP	
	L	L	H	H	BA,RA	ACT	Bank active / ILLEGAL	2
	L	L	H	L	BA,A10	PRE/PALL	Precharge / Precharge all banks	
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC	MRS	ILLEGAL	
Read	H	X	X	X	X	DESL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	Terminate burst	
	L	H	L	H	BA,CA,A10	RD/RDA	Terminate burst, begin read, determine AP	3
	L	H	L	L	BA,CA,A10	WR/WRA	Terminate burst, begin write, determine AP	3
	L	L	H	H	BA,RA	ACT	Bank active / ILLEGAL	2
	L	L	H	L	BA,A10	PRE/PALL	Terminate burst, precharge	
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC	MRS	ILLEGAL	
Write	H	X	X	X	X	DESL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	Terminate burst	
	L	H	L	H	BA,CA,A10	RD/RDA	Terminate burst, begin read, determine AP	3
	L	H	L	L	BA,CA,A10	WR/WRA	Terminate burst, begin write, determine AP	3
	L	L	H	H	BA,RA	ACT	Bank active / ILLEGAL	2
	L	L	H	L	BA,A10	PRE/PALL	Terminate burst, precharge	
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC	MRS	ILLEGAL	
Read with auto precharge	H	X	X	X	X	DESL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	RD/RDA	Support concurrent auto-precharge	2
	L	H	L	L	BA,CA,A10	WR/WRA	Support concurrent auto-precharge	2
	L	L	H	H	BA,RA	ACT	Bank active / ILLEGAL	2
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC	MRS	ILLEGAL	
Write with auto precharge	H	X	X	X	X	DESL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	RD/RDA	Support concurrent auto-precharge	2
	L	H	L	L	BA,CA,A10	WR/WRA	Support concurrent auto-precharge	2
	L	L	H	H	BA,RA	ACT	Bank active / ILLEGAL	2
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC	MRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	/Address	Command	Action	Notes
Precharging	H	X	X	X	X	DESL	NOP, idle after tRP	
	L	H	H	H	X	NOP	NOP, idle after tRP	
	L	H	H	L	X	BST	ILLEGAL	2
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	2
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	2
	L	L	H	H	BA,RA	ACT	Bank active / ILLEGAL	2
	L	L	H	L	BA,A10	PRE/PALL	Nop, idle after tRP	4
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC	MRS	ILLEGAL	
Row activating	H	X	X	X	X	DESL	NOP, row active after tRCD	
	L	H	H	H	X	NOP	NOP, row active after tRCD	
	L	H	H	L	X	BST	ILLEGAL	2
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	2
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	2
	L	L	H	H	BA,RA	ACT	ILLEGAL	2
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC	MRS	ILLEGAL	
Write recovering	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	ILLEGAL	2
	L	H	L	H	BA,CA,A10	RD/RDA	Begin read, determine AP	
	L	H	L	L	BA,CA,A10	WR/WRA	Begin write, determine AP	
	L	L	H	H	BA,RA	ACT	ILLEGAL	2
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC	MRS	ILLEGAL	
Refreshing	H	X	X	X	X	DESL	NOP, idle after tARFC	
	L	H	H	H	X	NOP	NOP, idle after tARFC	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	
	L	L	H	H	BA,RA	ACT	ILLEGAL	
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC	MRS	ILLEGAL	
Mode register accessing	H	X	X	X	X	DESL	NOP, idle after tMRD	
	L	H	H	H	X	NOP	NOP, idle after tMRD	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	
	L	L	H	H	BA,RA	ACT	ILLEGAL	
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC	MRS	ILLEGAL	

Notes:

1. All entries assumes that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to the bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.
   ILLEGAL: Device operation and/or data-integrity are not guaranteed.

Mode Register Field Table to Program Modes (Register Programmed with Normal MRS)

Address	BA0	BA1	A12	A11	A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	0	0	0	0	0	WB	0	0	CAS Latency			BT	Burst Length		

MRS Mode

CAS Latency				Burst Type		Burst Length					Write Burst Mode	
A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1	A9	Type
0	0	0	Reserved	0	Sequential	0	0	0	1	1	0	Programmed Burst Length
0	0	1	Reserved	1	Interleave	0	0	1	2	2	1	Single Location Access
0	1	0	2			0	1	0	4	4		
0	1	1	3			0	1	1	8	8		
1	0	0	Reserved			1	0	0	Reserved	Reserved		
1	0	1	Reserved			1	0	1	Reserved	Reserved		
1	1	0	Reserved			1	1	0	Reserved	Reserved		
1	1	1	Reserved			1	1	1	Full Page	Reserved		

Burst Sequence

BURST LENGTH	STARTING COLUMN ADDRESS	ORDER OF ACCESSES WITHIN A BURST	
		TYPE=SEQUENTIAL	TYPE=INTERLEAVED
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	N=A0 - A9 (x8) N=A0 - A8 (x16) (location 0 – y)	Cn, Cn+1, Cn+2, Cn+3, Cn+4..., …Cn-1, Cn…	Not Supported

Notes:

1. For full-page accesses: y = 1023 (x8), 511 (x16).
2. For a burst length of two, A1–A9(A8) select the block-of-two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2–A9(A8) select the block-of-four burst; A0–A1 select the starting column within the block.
4. For a burst length of eight, A3–A9(A8) select the block-of-eight burst; A0–A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0–A9(A8) select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For a burst length of one, A0–A9(A8) select the unique column to be accessed, and mode register bit A3 is ignored.

Power-up sequence

Power-up sequence

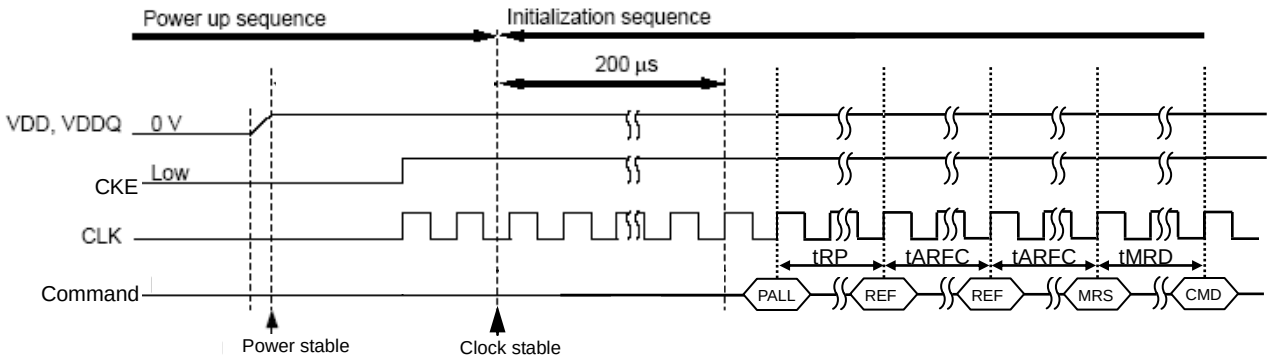
1. Apply VDD and VDDQ at the same time. Keep CKE low during power up.
2. Wait for stable power.
3. Start clock and drive CKE high.

Note: Voltage on any input pin must not exceed Vdd+0.3V during power up.

Initialization sequence

4. After stable power and stable clock, wait 200us.
5. Issue precharge all command (PALL).
6. After tRP delay, set 2 or more auto refresh commands (REF).
7. Set the mode register set command (MRS) to initialize the mode register.

Note: We recommend that you keep DQM and CKE high during initialization sequence to prevent data contention on the DQ bus.



Power-up sequence and Initialization sequence

Operation of the SDRAM

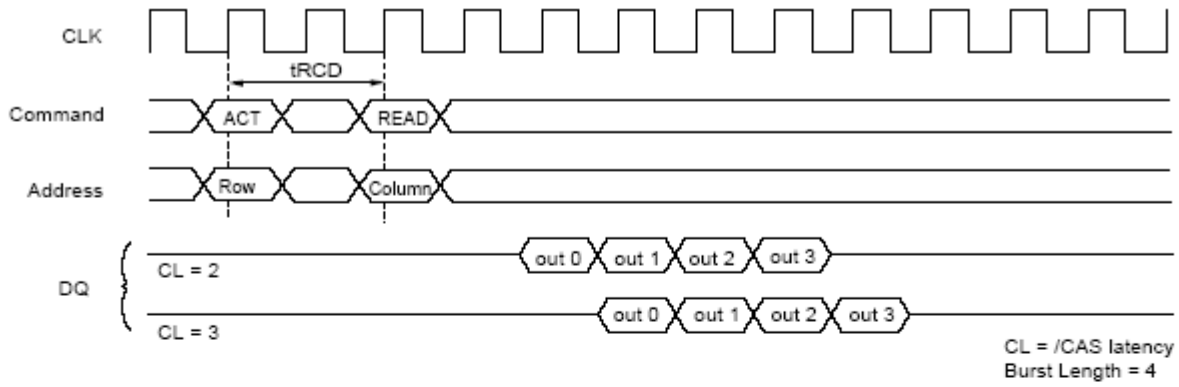
Read/Write Operations

Bank active

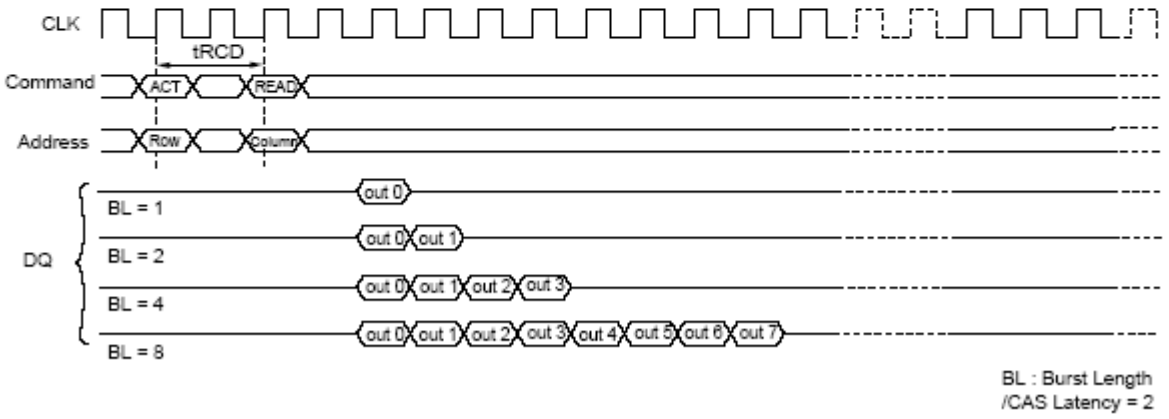
Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACT) command. An interval of tRCD is required between the bank active command input and the following read/write command input.

Read operation

A read operation starts when a read command is input. Output buffer becomes Low-Z in the (CAS Latency - 1) cycle after read command set. The SDRAM can perform a burst read operation.
The burst length can be set to 1, 2, 4 and 8. The start address for a burst read is specified by the column address and the bank select address at the read command set cycle. In a read operation, data output starts after the number of clocks specified by the CAS Latency. The CAS Latency can be set to 2 or 3.
When the burst length is 1, 2, 4 and 8 the DOUT buffer automatically becomes High-Z at the next clock after the successive burst-length data has been output.
The CAS latency and burst length must be specified at the mode register.



/CAS Latency



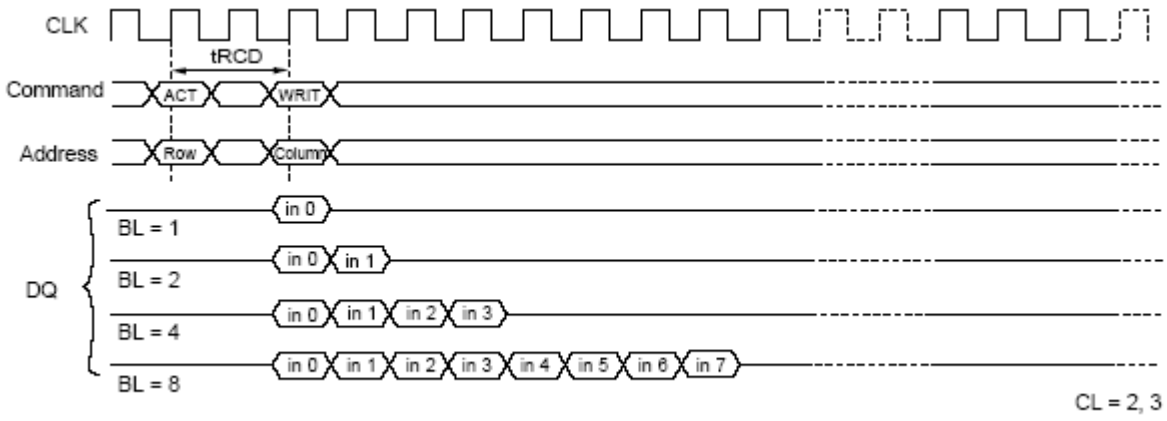
Burst Length

Write operation

Burst write or single write mode is selected

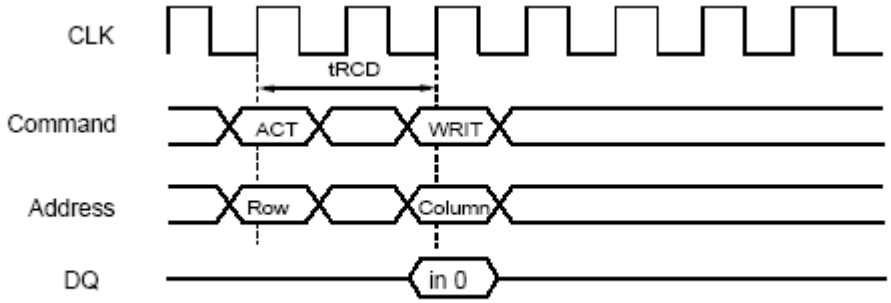
1. Burst write: A burst write operation is enabled by setting OPCODE A9 to 0. A burst write starts in the same clock as a write command set. (The latency of data input is 0 clock.) The burst length can be set to 1, 2, 4 and 8, like burst read operations. The write start address is specified by the column address and the bank select address at the write command set cycle.

.



Burst write

2. Single write: A single write operation is enabled by setting OPCODE A9 to 1. In a single write operation, data is only written to the column address and the bank select address specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0 clock).



Single write

Auto Precharge

Read with auto-precharge

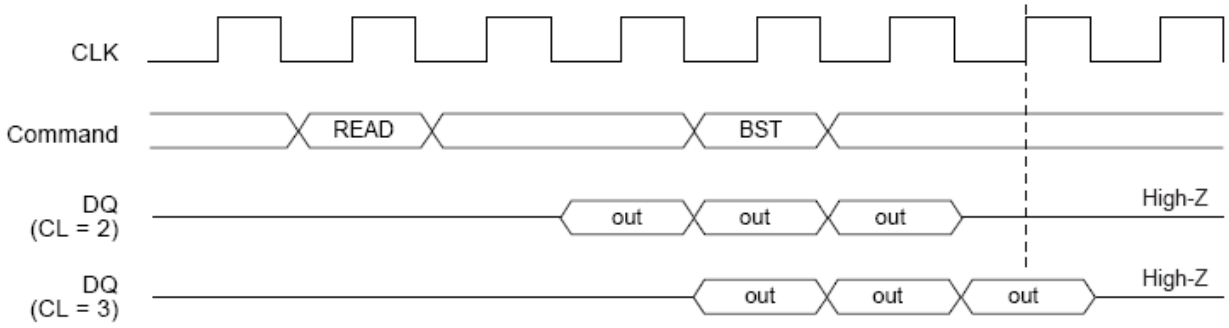
In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACT) command.
The next ACT command can be issued at the later time of either tRP after internal precharge or tRC after the previous ACT.

Write with auto-precharge

In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation. The command executed for the same bank after the execution of this command must be the bank active (ACT) command.
The next ACT command can be issued at the later time of either tDAL from the last input data cycle or tRC after the previous ACT.

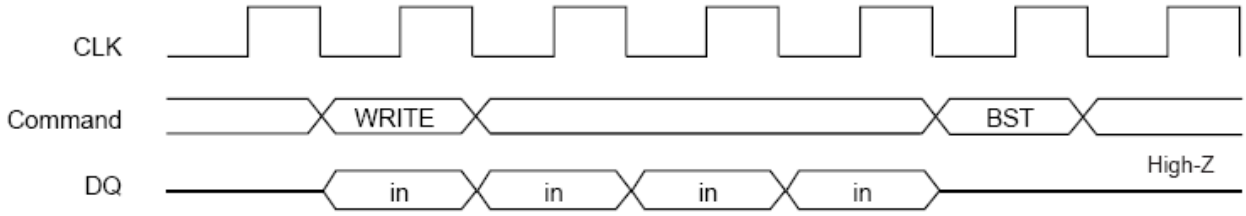
Burst Stop Command

During a read cycle, when the burst stop command is issued, the burst read data are terminated and the data bus goes to High-Z after the CAS latency from the burst stop command.



Burst Stop at Read

During a write cycle, when the burst stop command is issued, the burst write data are terminated and data bus goes to High-Z at the same clock with the burst stop command.

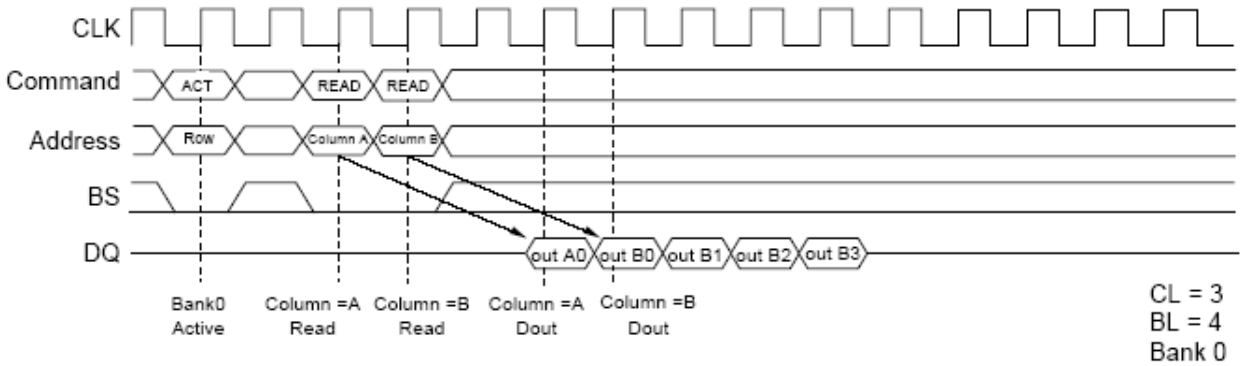


Burst Stop at Write

Command Intervals

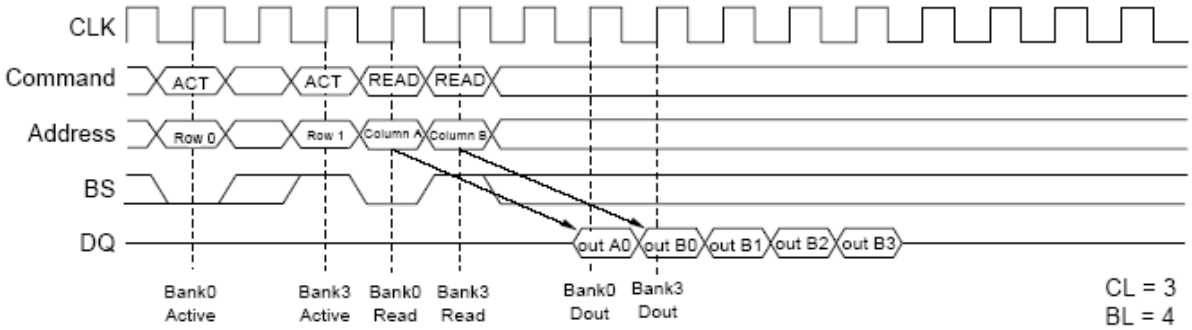
Read command to Read command interval

1. Same bank, same ROW address: When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 clock. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.



READ to READ Command Interval (same ROW address in same bank)

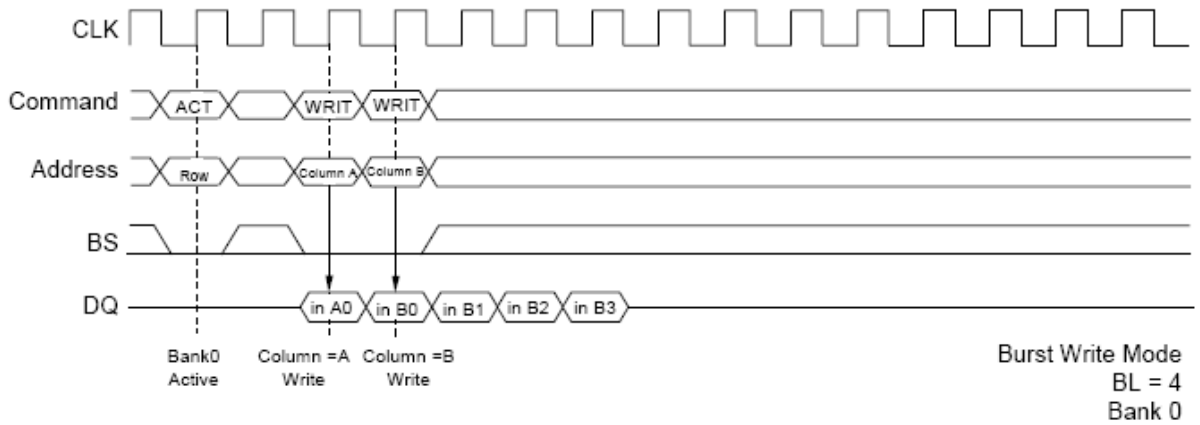
2. Same bank, different ROW address: When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the second read can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.



READ to READ Command Interval (different bank)

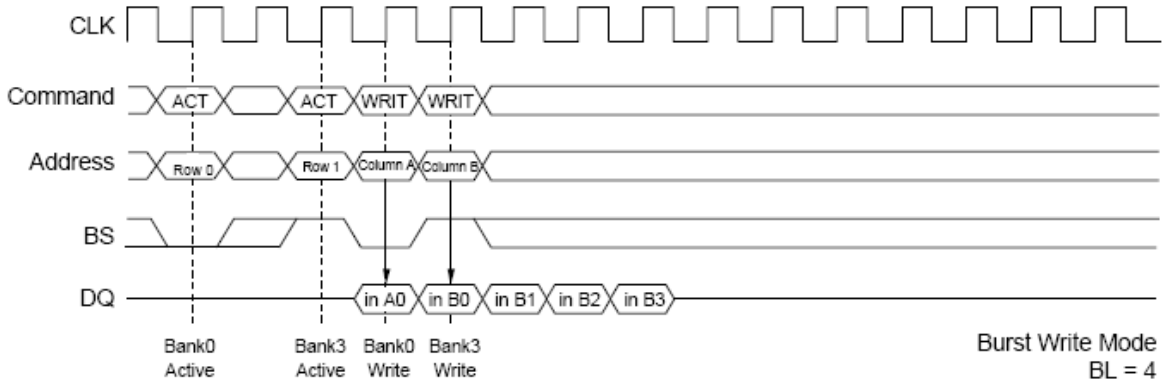
Write command to Write command interval

1. Same bank, same ROW address: When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 clock. In the case of burst writes, the second write command has priority.



WRITE to WRITE Command Interval (same ROW address in same bank)

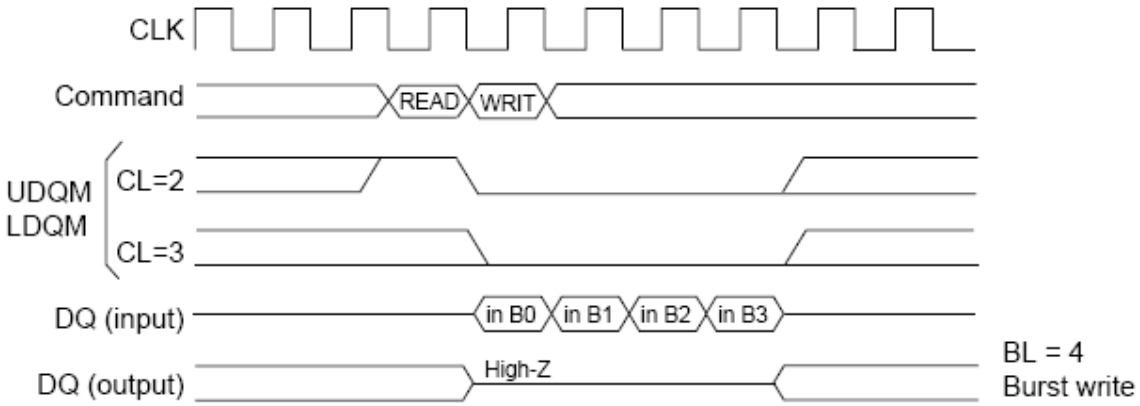
2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the second write can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. In the case of burst write, the second write command has priority.



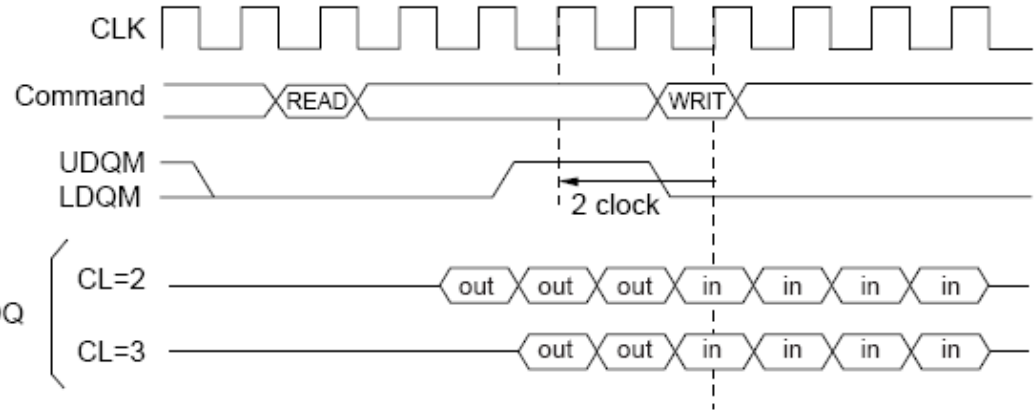
WRITE to WRITE Command Interval (different bank)

Read command to Write command interval

1. Same bank, same ROW address: When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 clock. However, UDQM and LDQM must be set High so that the output buffer becomes High-Z before data input.



READ to WRITE Command Interval (1)

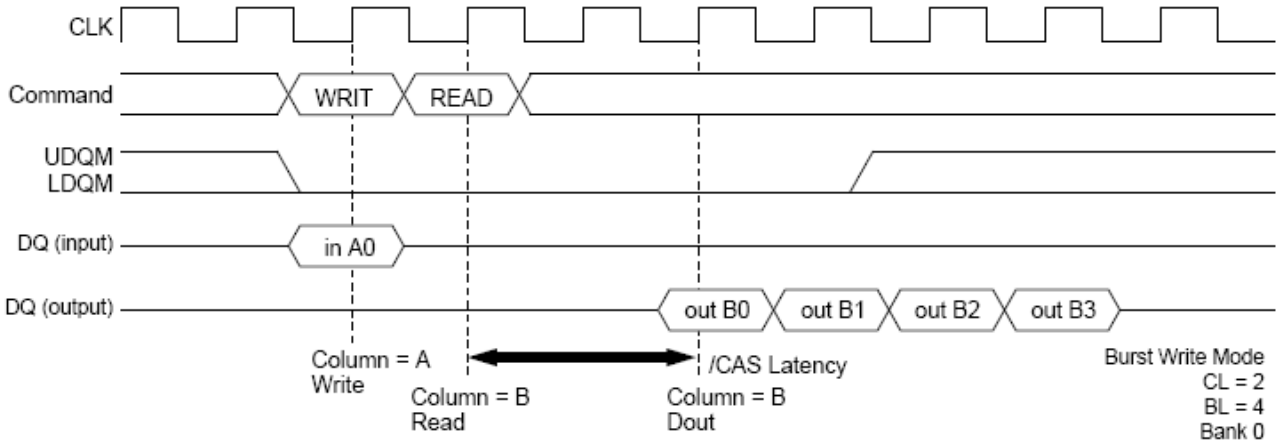


READ to WRITE Command Interval (2)

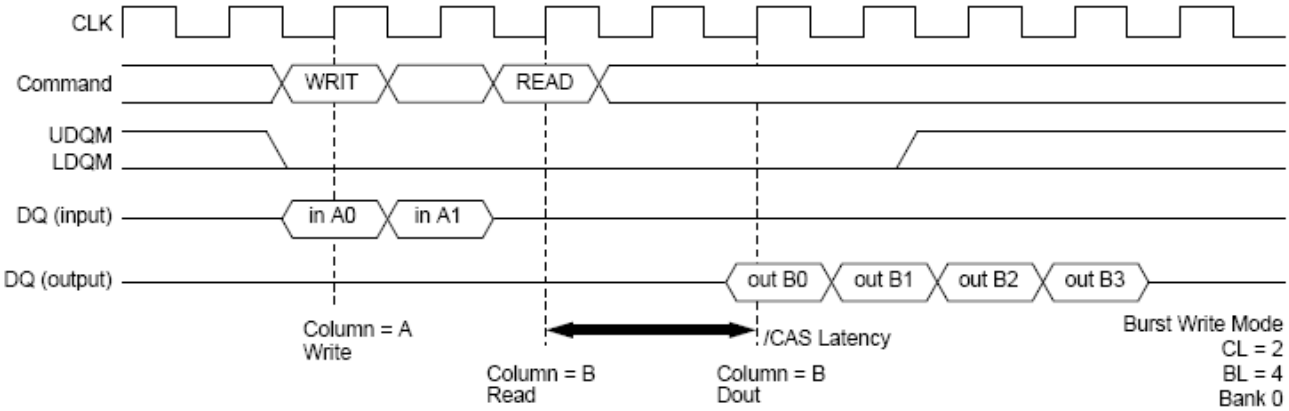
2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank active state. However, UDQM and LDQM must be set High so that the output buffer becomes High-Z before data input.

Write command to Read command interval:

1. Same bank, same ROW address: When the read command is executed at the same ROW address of the same bank as the preceding write command, the read command can be performed after an interval of no less than 1 clock. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed.



WRITE to READ Command Interval (1)

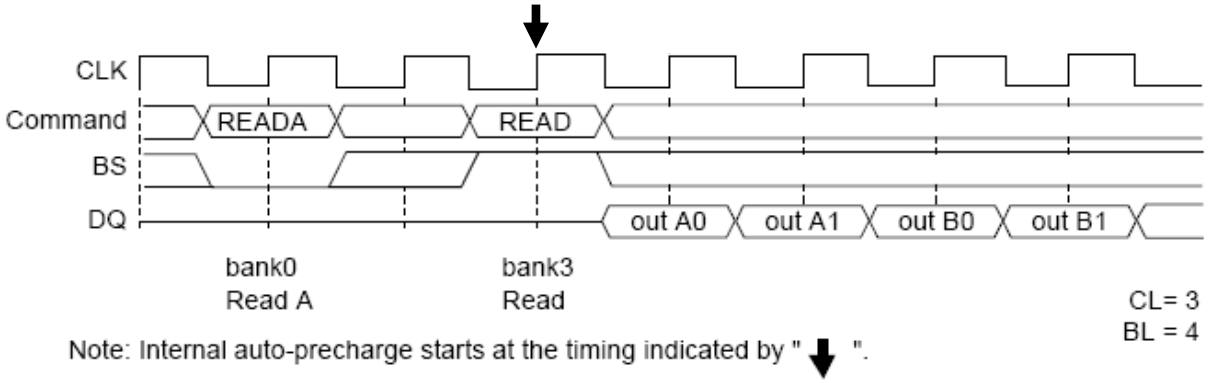


WRITE to READ Command Interval (2)

2. Same bank, different ROW address: When the ROW address changes, consecutive read commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the read command can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed (as in the case of the same bank and the same address).

Read with auto precharge to Read command interval (concurrent auto-precharge)

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. Even when the first read with auto-precharge is a burst read that is not yet finished, the data read by the second command is valid. The internal auto-precharge of one bank starts at the clock of the second command.

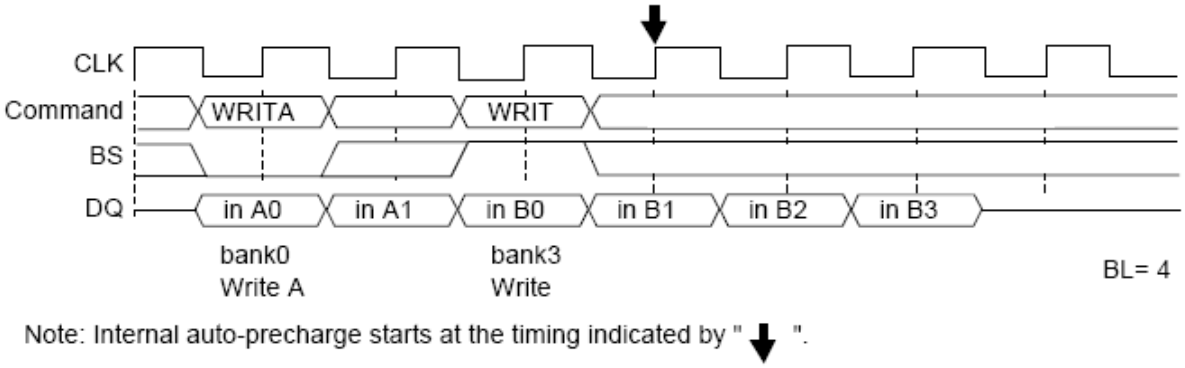


Read with Auto Precharge to Read Command Interval (Different bank)

2. Same bank: The consecutive read command (the same bank) is illegal.

Write with auto precharge to Write command interval (concurrent auto-precharge)

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. In the case of burst writes, the second write command has priority. The internal auto-precharge of one bank starts at the next clock of the second command.

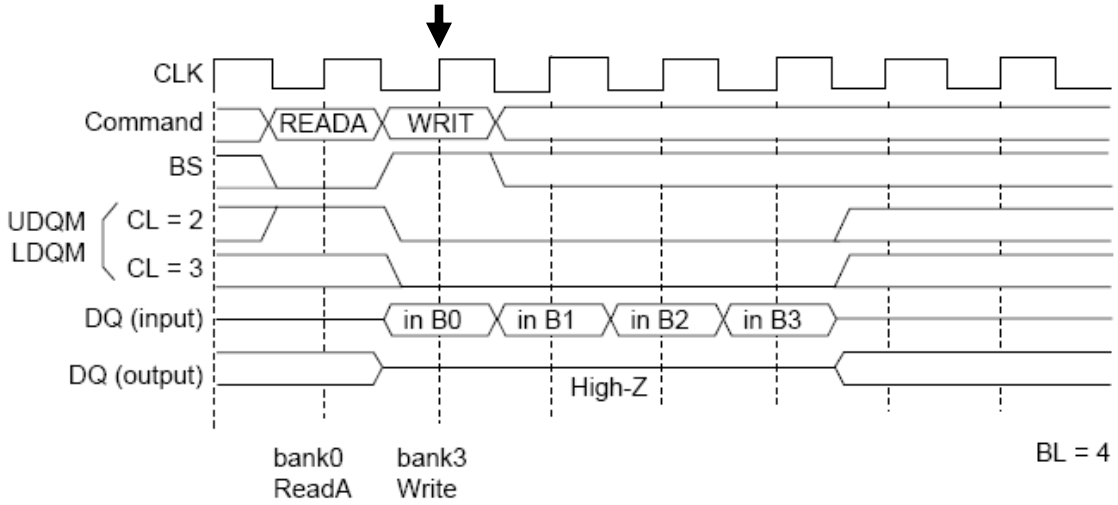


Write with Auto Precharge to Write Command Interval (Different bank)

2. Same bank: The consecutive write command (the same bank) is illegal.

Read with auto precharge to Write command interval (concurrent auto-precharge)

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. However, UDQM and LDQM must be set High so that the output buffer becomes High-Z before data input. The internal auto-precharge of one bank starts at the clock of the second command.



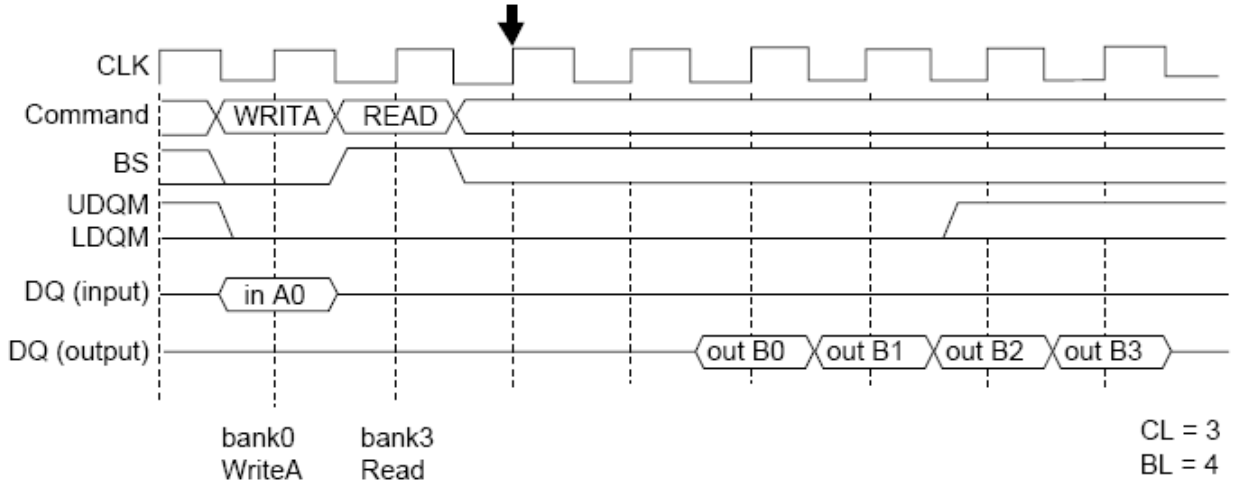
Note: Internal auto-precharge starts at the timing indicated by " ".

Read with Auto Precharge to Write Command Interval (Different bank)

2. Same bank: The consecutive write command from read with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

Write with auto precharge to Read command interval (concurrent auto-precharge)

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. However, in case of a burst write, data will continue to be written until one clock before the read command is executed. The internal auto-precharge of one bank starts at the next clock of the second command.



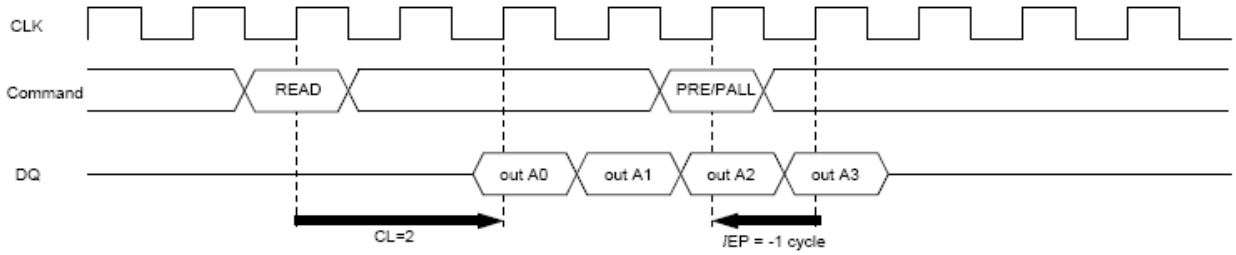
Note: Internal auto-precharge starts at the timing indicated by " ".

Write with Auto Precharge to Read Command Interval (Different bank)

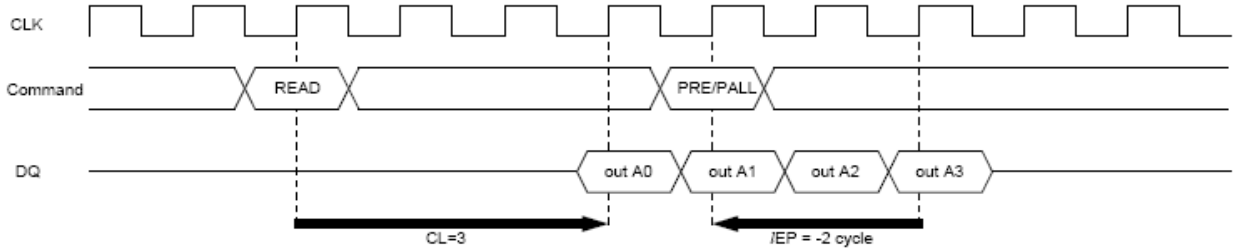
2. Same bank: The consecutive read command from write with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

Read command to Precharge command interval (same bank)

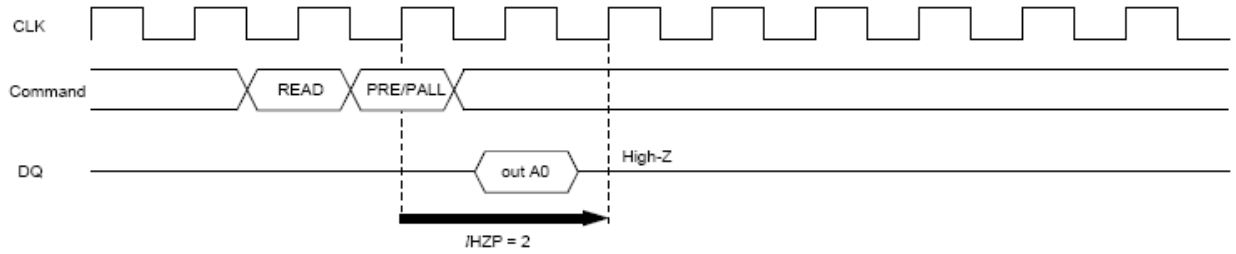
When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one clock. However, since the output buffer then becomes High-Z after the clocks defined by *l*HZP, there is a case of interruption to burst read data output will be interrupted, if the precharge command is input during burst read. To read all data by burst read, the clocks defined by *l*EP must be assured as an interval from the final data output to precharge command execution.



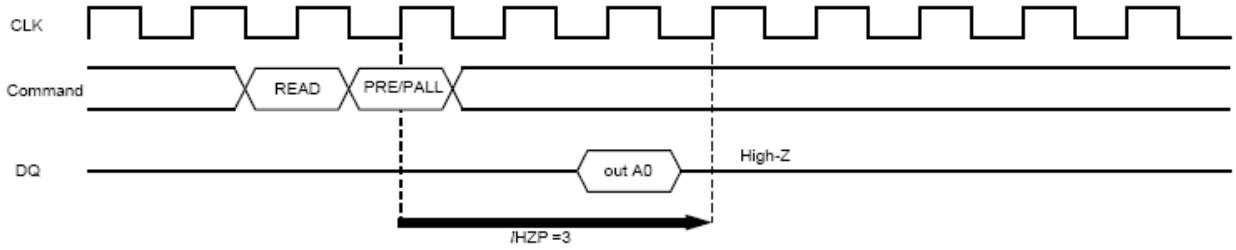
READ to PRECHARGE Command Interval (same bank): To output all data (CL = 2, BL = 4)



READ to PRECHARGE Command Interval (same bank): To output all data (CL = 3, BL = 4)



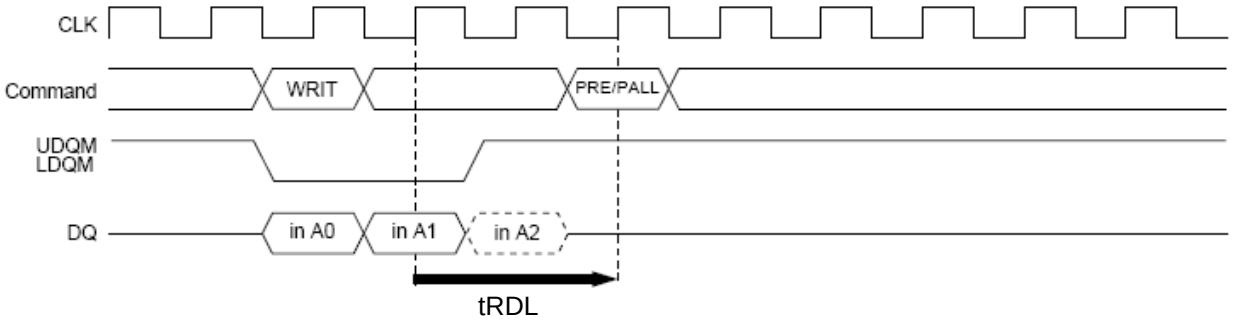
READ to PRECHARGE Command Interval (same bank): To stop output data (CL = 2, BL = 1, 2, 4, 8)



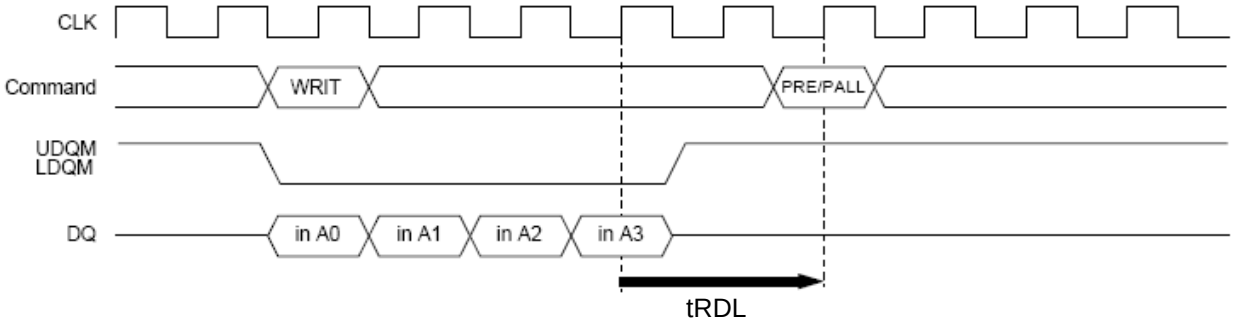
READ to PRECHARGE Command Interval (same bank): To stop output data (CL = 3, BL = 1, 2, 4, 8)

Write command to Precharge command interval (same bank)

When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 clock. However, if the burst write operation is unfinished, the input data must be masked by means of UDQM and LDQM for assurance of the clock defined by tRDL.



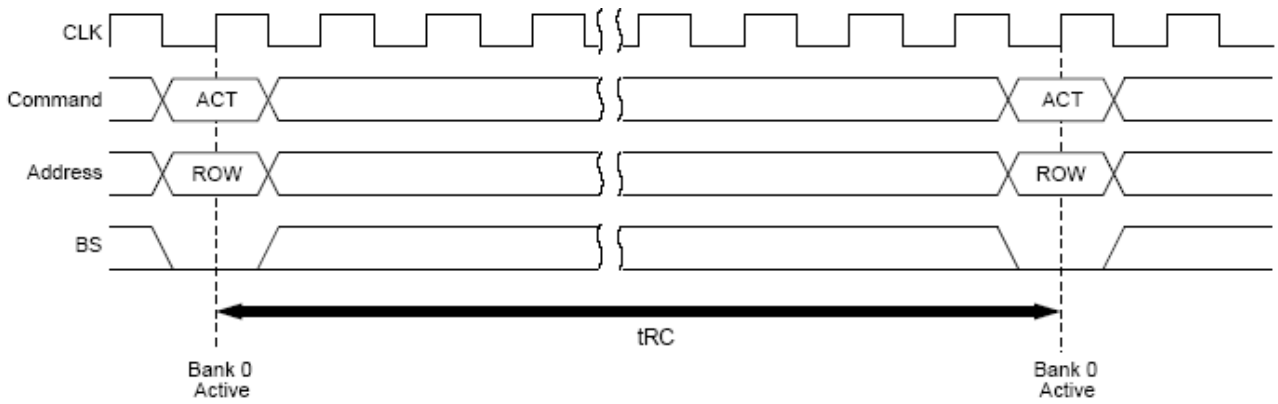
WRITE to PRECHARGE Command Interval (same bank) (BL = 4 (To stop write operation))



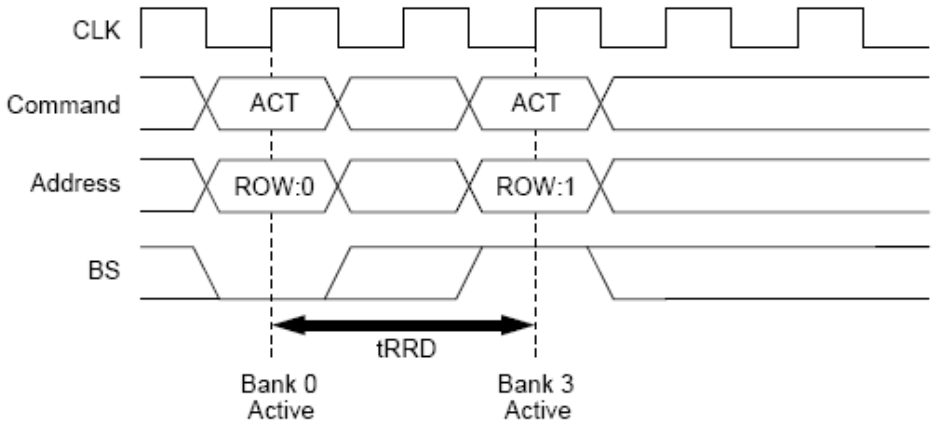
WRITE to PRECHARGE Command Interval (same bank) (BL = 4 (To write all data))

Bank active command interval

1. Same bank: The interval between the two bank active commands must be no less than t_{RC}.
2. In the case of different bank active commands: The interval between the two bank active commands must be no less than t_{RRD}.



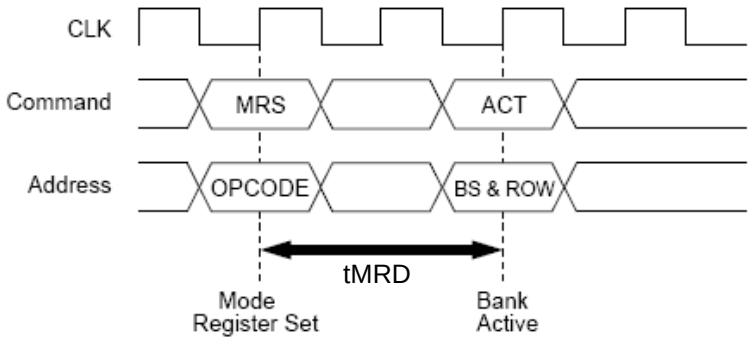
Bank Active to Bank Active for Same Bank



Bank Active to Bank Active for Different Bank

Mode register set to Bank active command interval

The interval between setting the mode register and executing a bank active command must be no less than t_{MRD}.



Mode register set to Bank active command interval

DQM Control

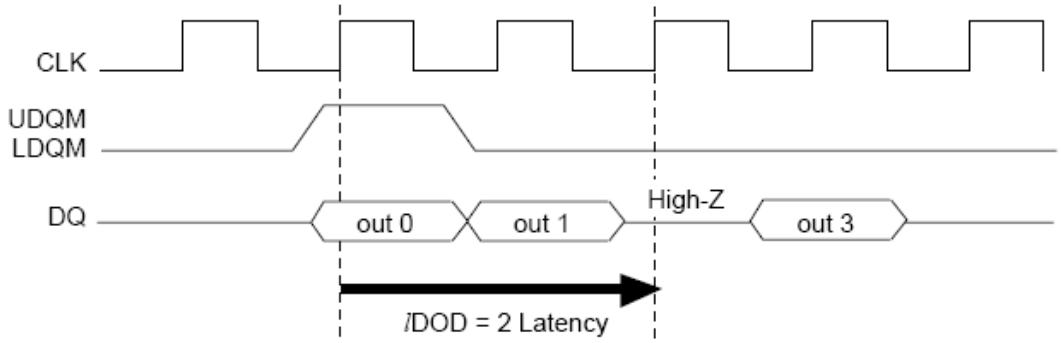
The UDQM and LDQM mask the upper and lower bytes of the DQ data, respectively. The timing of UDQM and LDQM is different during reading and writing.

Reading

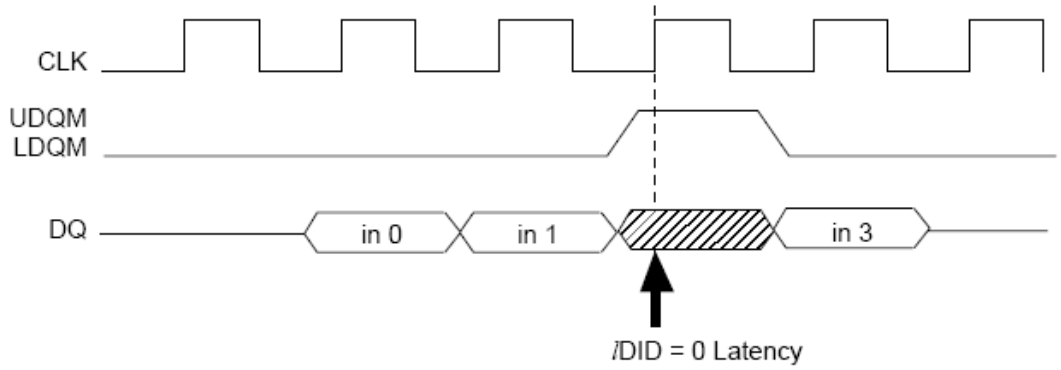
When data is read, the output buffer can be controlled by UDQM and LDQM. By setting UDQM and LDQM to Low, the output buffer becomes Low-Z, enabling data output. By setting UDQM and LDQM to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of UDQM and LDQM during reading is 2 clocks.

Writing

Input data can be masked by UDQM and LDQM. By setting DQM to Low, data can be written. In addition, when UDQM and LDQM are set to High, the corresponding data is not written, and the previous data is held. The latency of UDQM and LDQM during writing is 0 clock.



Reading



Writing

Refresh

Auto-refresh

All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the internal counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycles are required to refresh all the ROW addresses within tREF (max.). The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

Self-refresh

After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. Before and after self-refresh mode, execute auto-refresh to all refresh addresses in or within tREF(max.) period on the condition 1 and 2 below.

1. Enter self-refresh mode within time as below* after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
2. Start burst refresh or distributed refresh at equal interval to all refresh addresses within time as below* after exiting from self-refresh mode.

Note: tREF(max.) / refresh cycles.

Others

Power-down mode

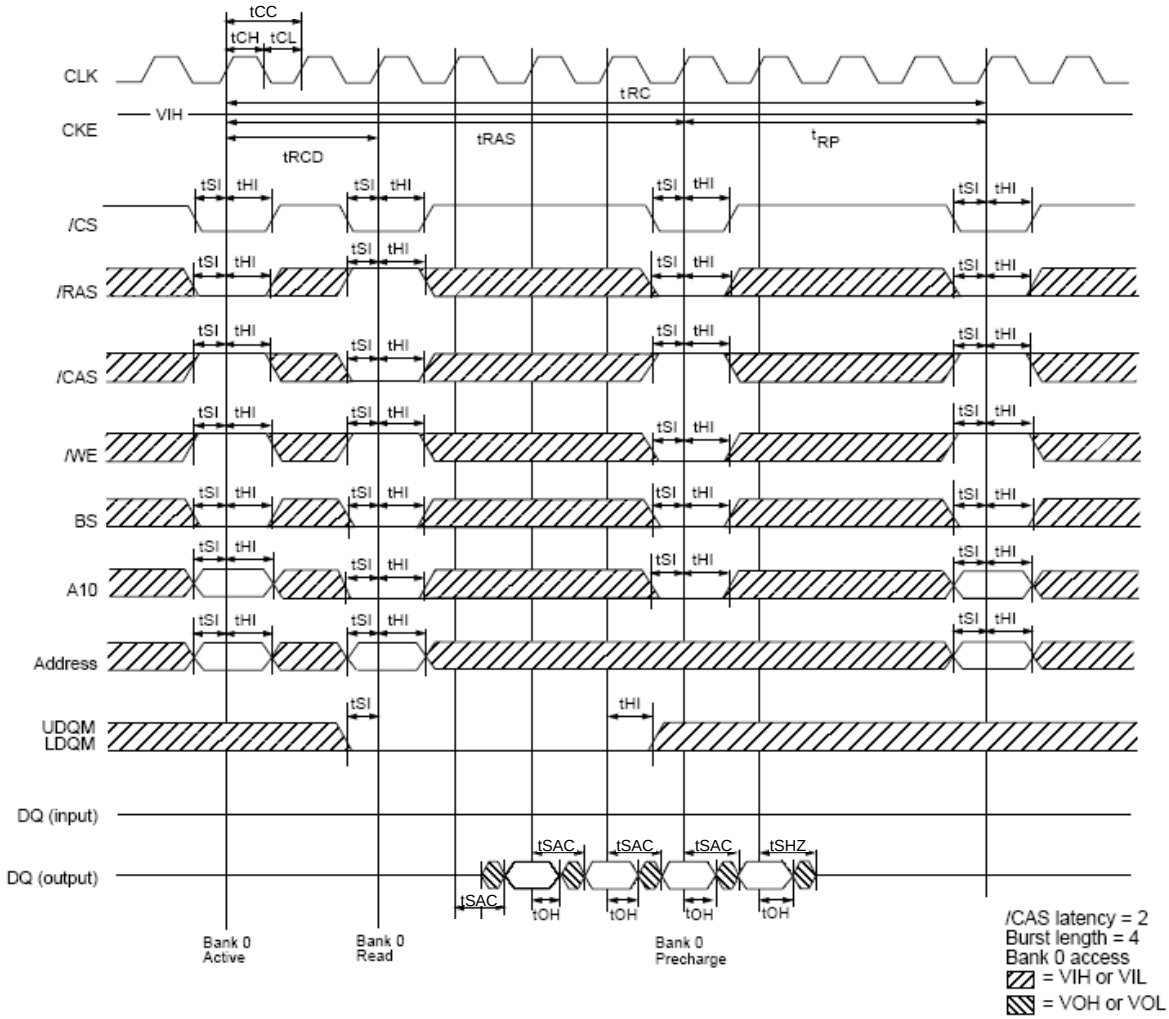
The SDRAM enters power-down mode when CKE goes Low. For cases of all banks in the IDLE state, it is referred to as precharge power-down mode. For cases of any bank in the ACTIVE state, it is referred to as active power-down mode. In power down mode, power consumption is suppressed by deactivating the input buffers excluding CLK and CKE. Power down mode continues while CKE is held Low. In addition, by setting CKE to High, the SDRAM exits from the power down mode, and command input is enabled from the next clock. In this mode, internal refresh is not performed.

Clock suspend mode

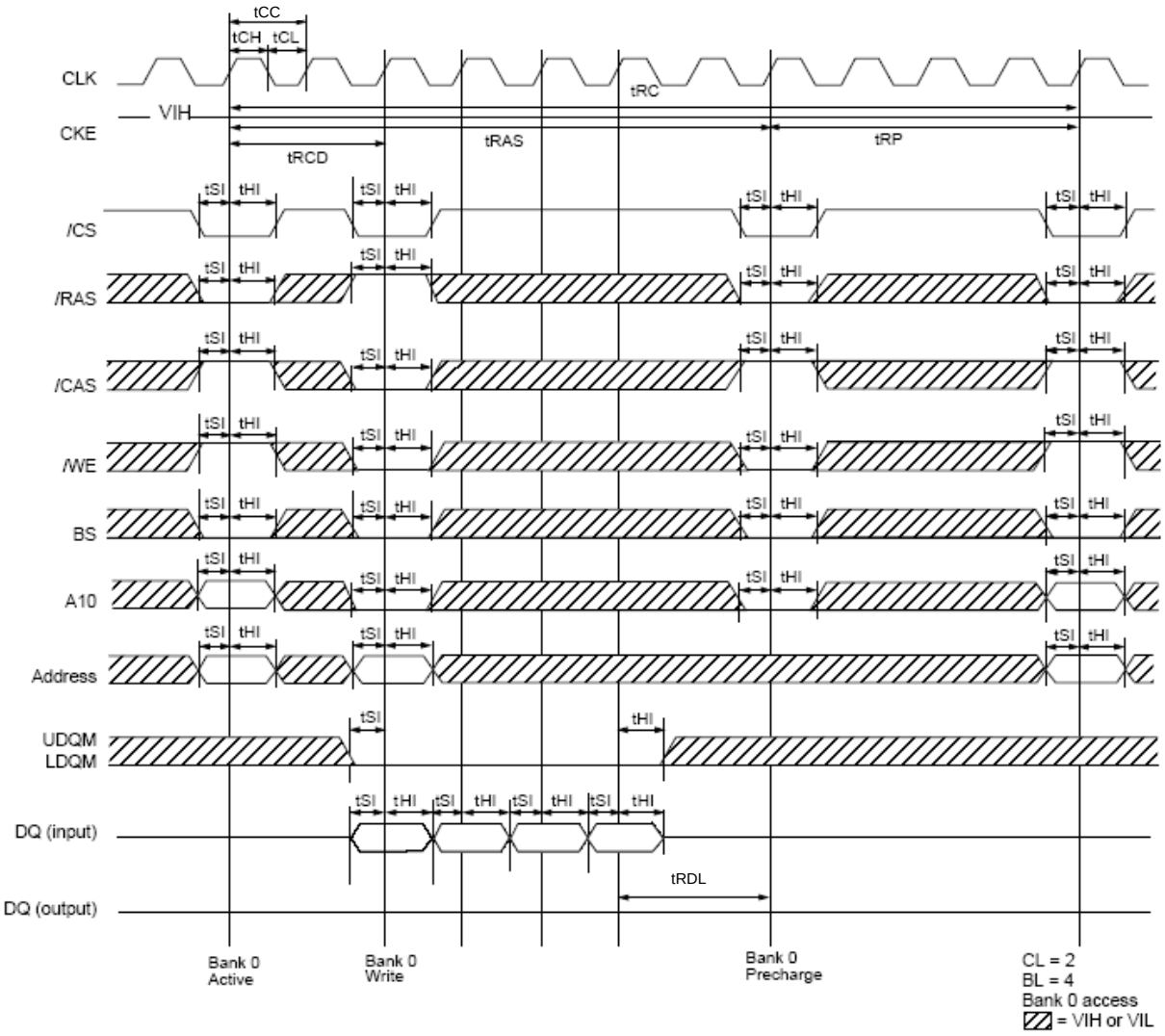
By driving CKE to Low during a bank active or read/write operation, the SDRAM enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE is driven High, the SDRAM terminates clock suspend mode, and command input is enabled from the next clock. For details, refer to the "CKE Truth Table".

Timing Waveforms

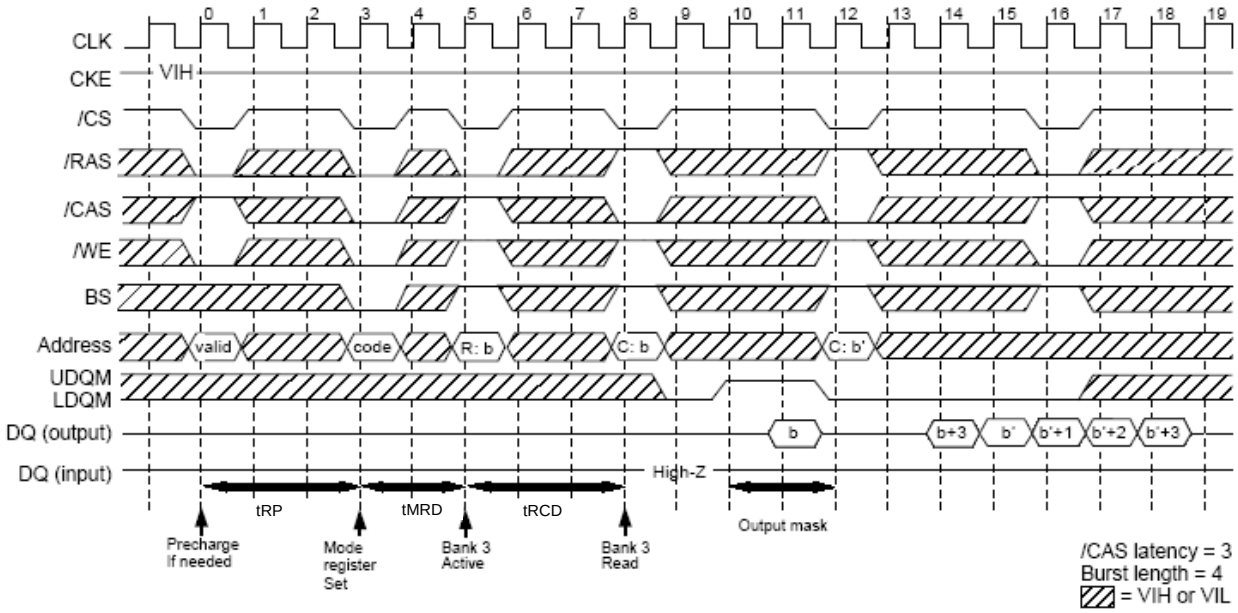
Read Cycle



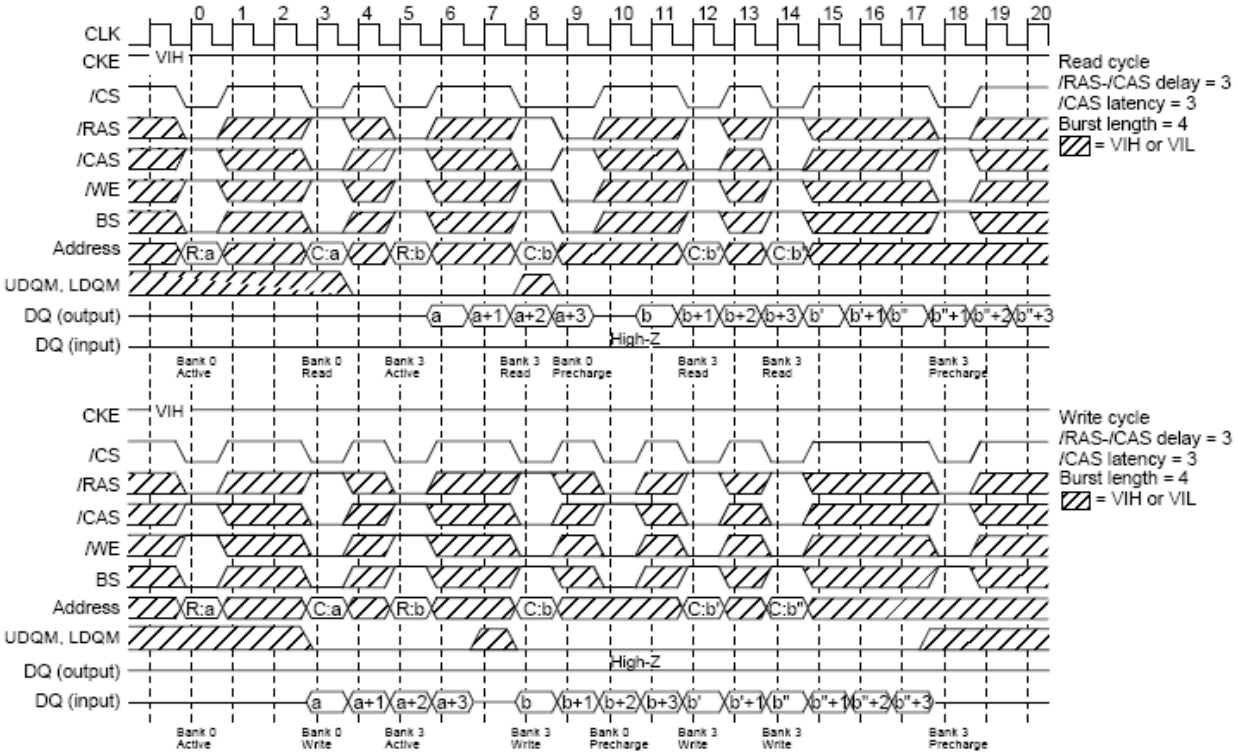
Write Cycle


tCC
tCH
tCL
CLK
tRC
VIH
CKE
tRAS
tRP
tRCD
tSI
tHI
/CS
/RAS
/CAS
/WE
BS
A10
Address
UDQM
LDQM
DQ (input)
tRDL
DQ (output)
Bank 0
Active
Bank 0
Write
Bank 0
Precharge
CL = 2
BL = 4
Bank 0 access
= VIH or VIL

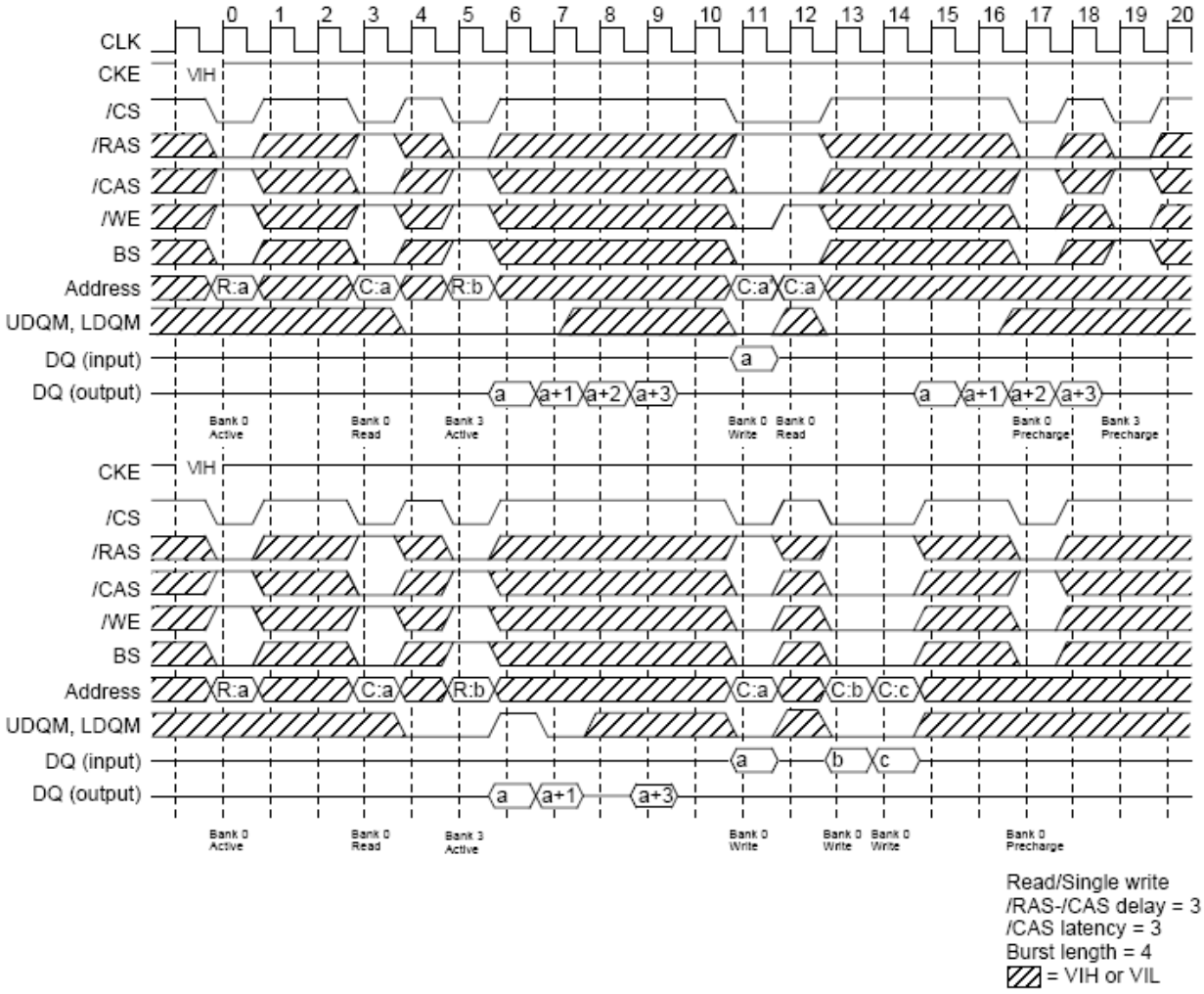
Mode Register Set Cycle



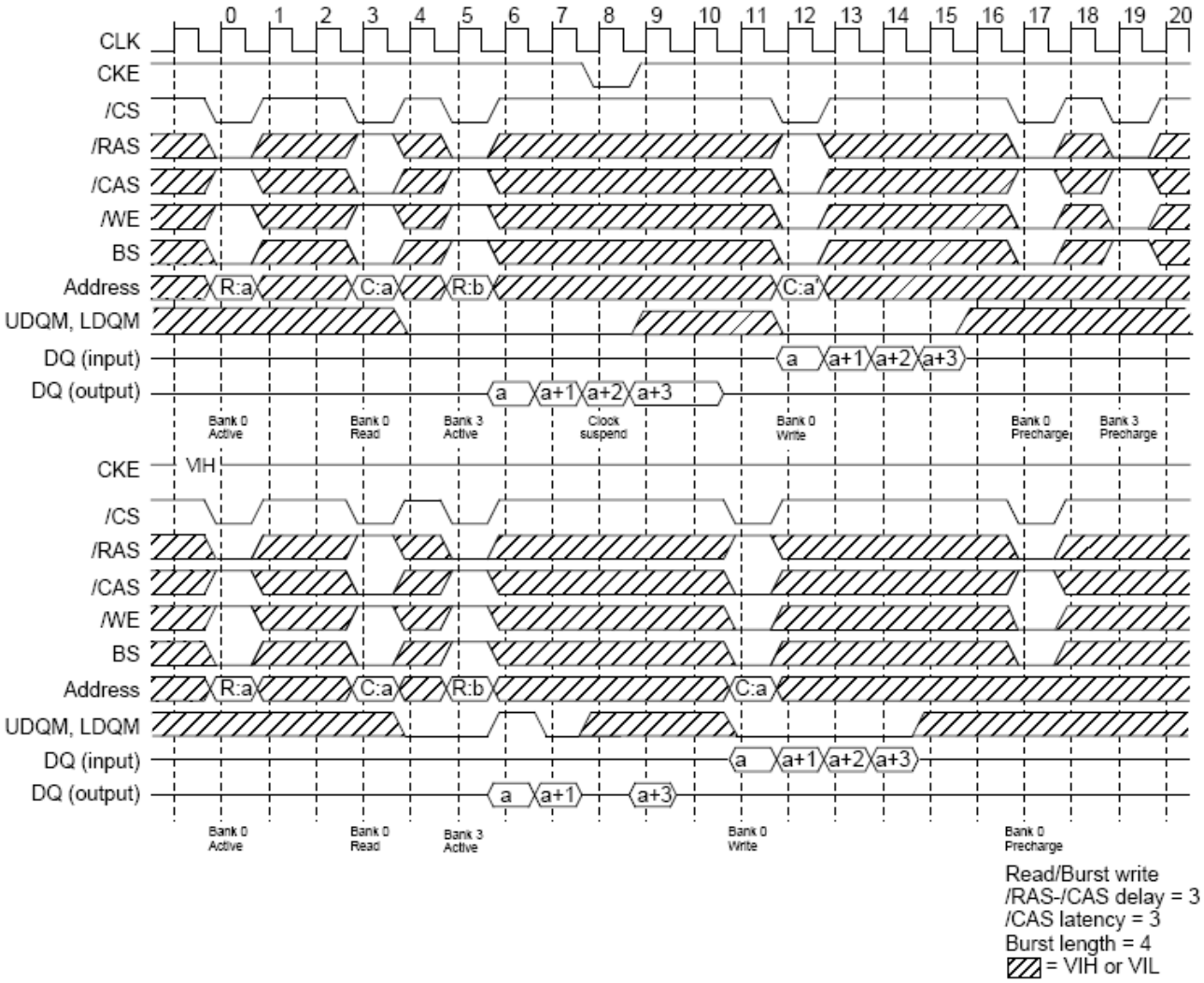
Read Cycle/Write Cycle



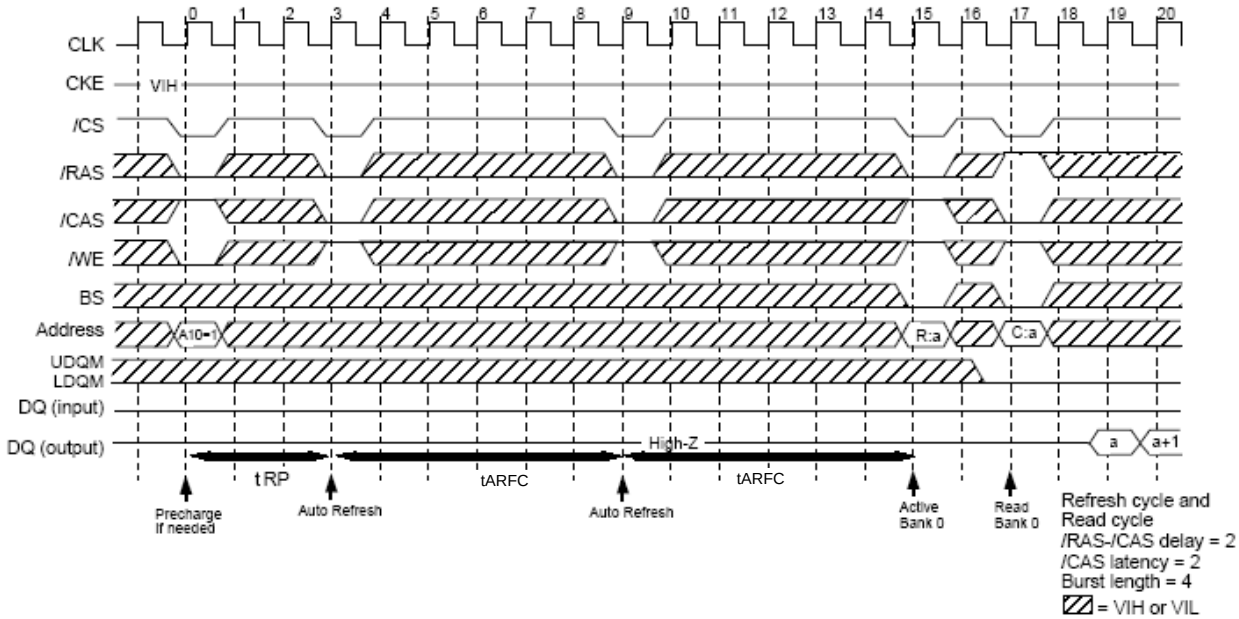
Read/Single Write Cycle



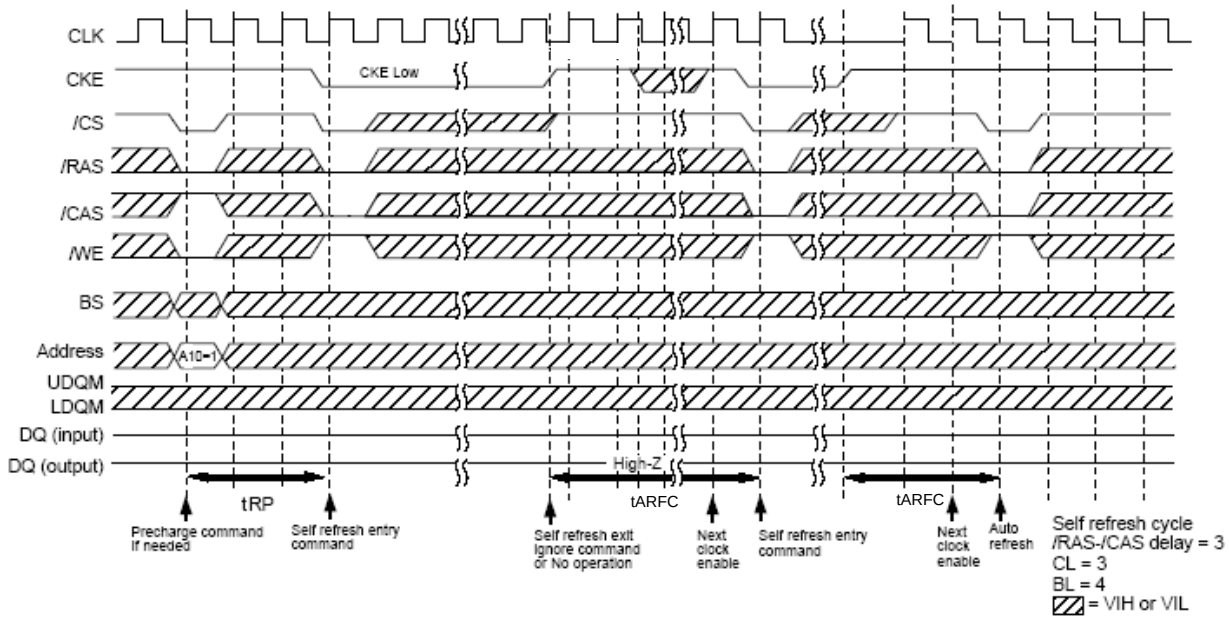
Read/Burst Write Cycle



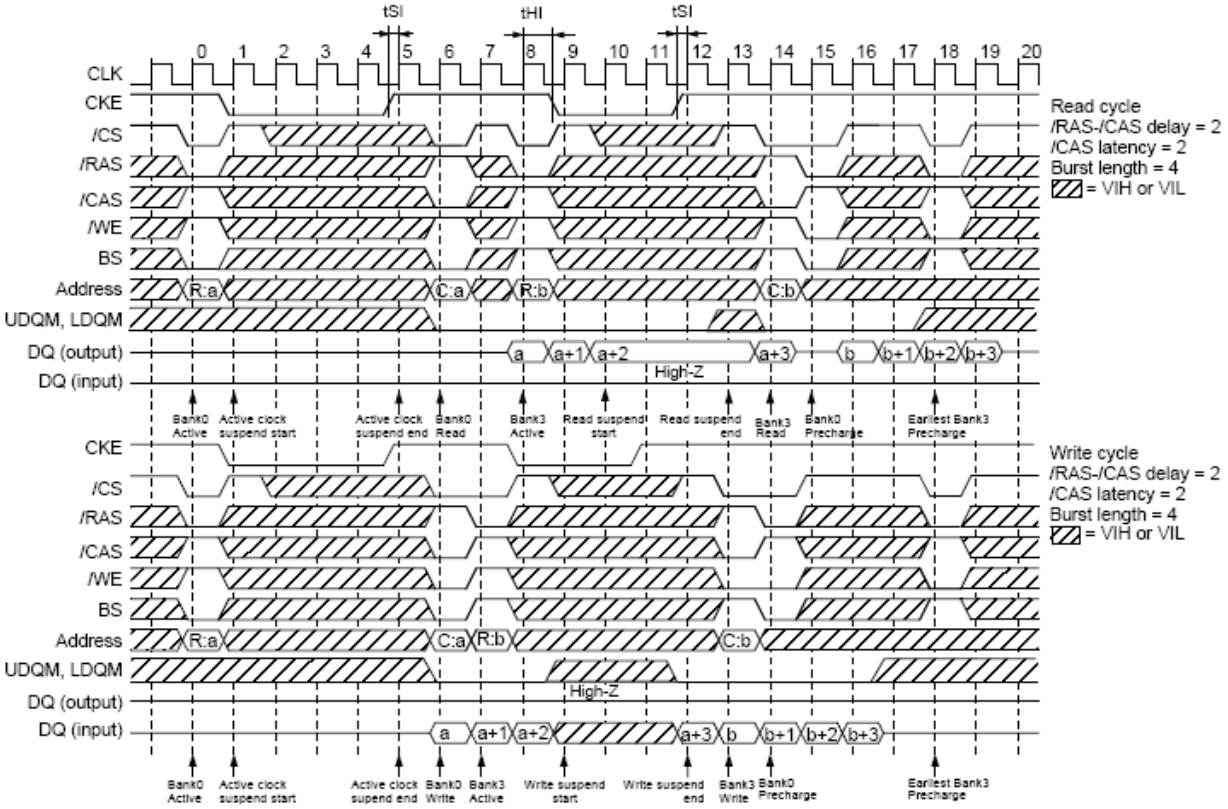
Auto Refresh Cycle



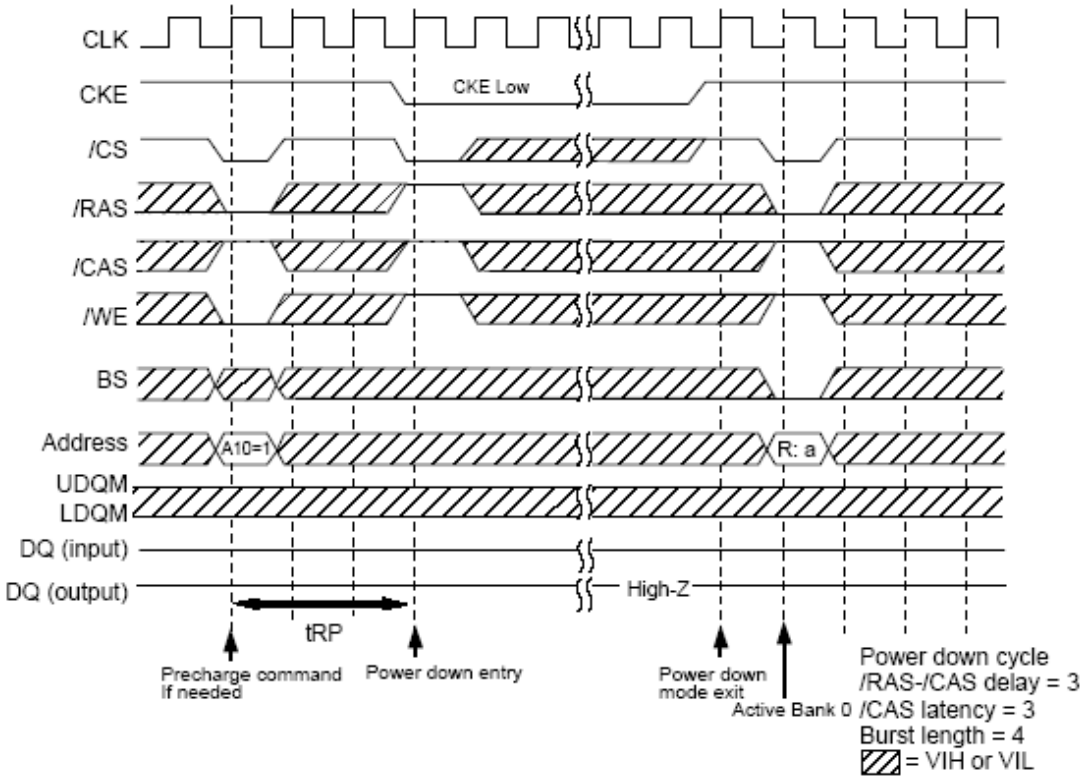
Self Refresh Cycle



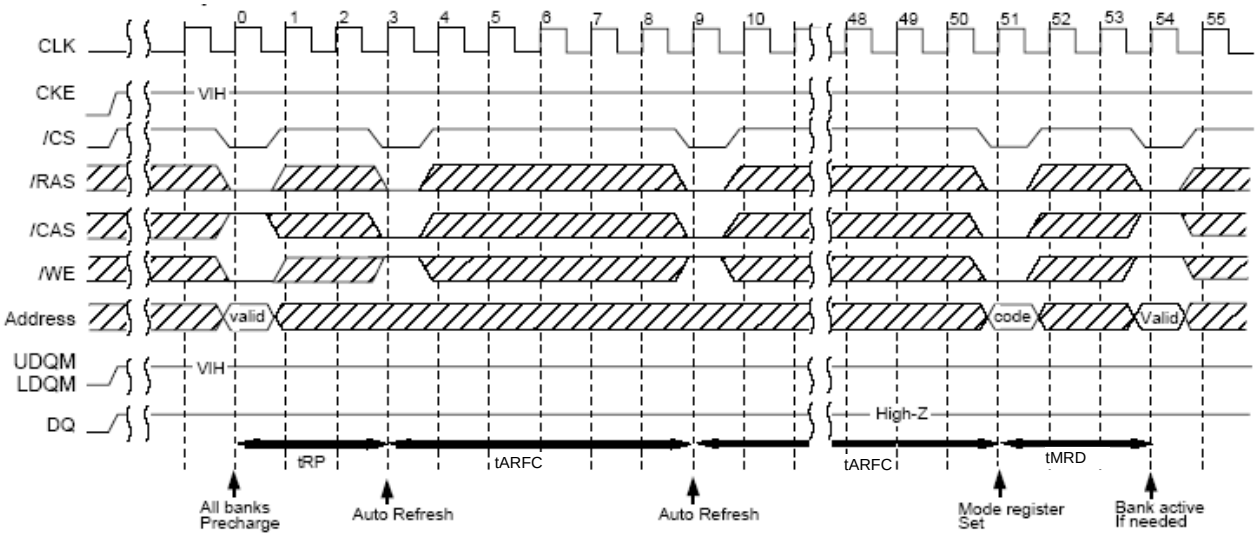
Active Power-Down Mode, Clock Suspend Mode



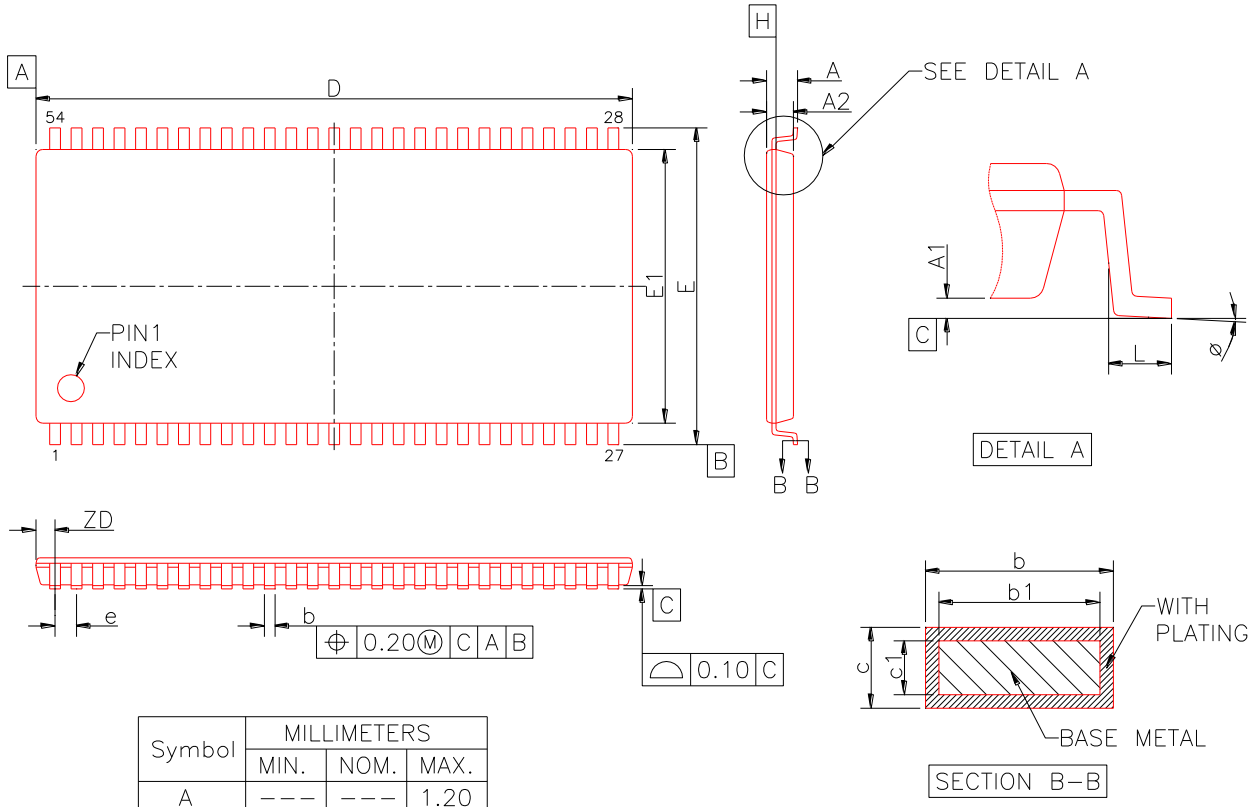
Precharge Power-Down Mode



Initialization Sequence



Package Drawing



Symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.05	---	0.15
A2	0.95	1.00	1.05
b	0.28	---	0.45
b1	0.25	---	0.40
c	0.12	---	0.21
c1	0.12	0.127	0.16
D	22.12	22.22	22.32
E	11.56	11.76	11.96
E1	10.06	10.16	10.26
L	0.40	0.50	0.60
e	0.80 BSC		
ø	0°	---	8°
ZD	0.71 REF		

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