128Mb DDR SDRAM Specification

A3S28D30FTP
A3S28D40FTP

Zentel Electronics Corp.

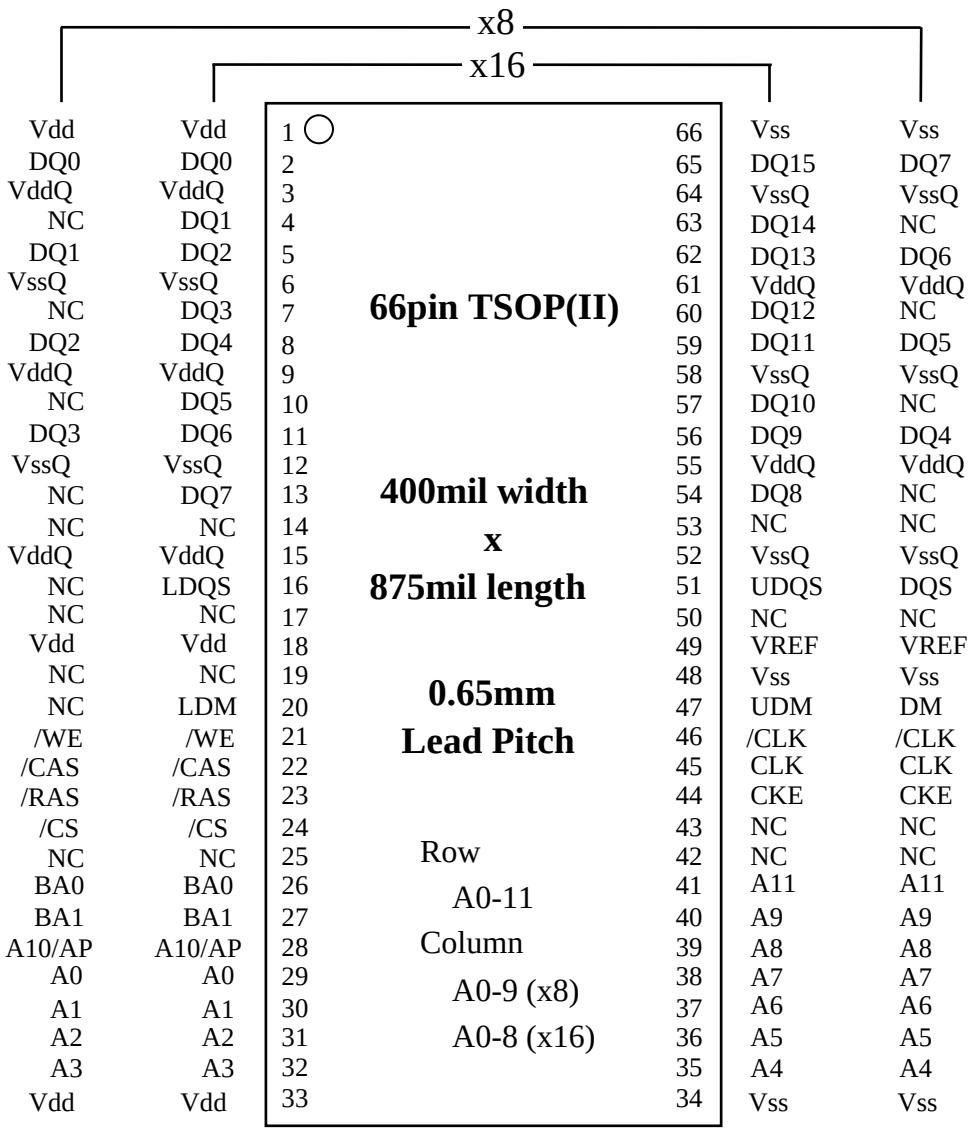
DESCRIPTION

A3S28D30FTP is a 4-bank x 4,194,304-word x 8bit, A3S28D40FTP is a 4-bank x 2,097,152-word x 16bit double data rate synchronous DRAM , with SSTL_2 interface. All control and address signals are referenced to the rising edge of CLK. Input data is registered on both edges of data strobe ,and output data and data strobe are referenced on both edges of CLK. The A3S28D30/40FTP achieves very high speed clock rate up to 250 MHz .

FEATURES

- Vdd=VddQ=2.5V±0.2V (-4, -5E, -5)
- Double data rate architecture ; two data transfers per clock cycle.
- Bidirectional , data strobe (DQS) is transmitted/received with data
- Differential clock input (CLK and /CLK)
- DLL aligns DQ and DQS transitions with CLK transitions edges of DQS
- Commands entered on each positive CLK edge ;
- Data and data mask referenced to both edges of DQS
- 4 bank operation controlled by BA0 , BA1 (Bank Address)
- /CAS latency - 2.0 / 2.5 / 3.0 / 4.0 (programmable) ;
  Burst length - 2 / 4 / 8 (programmable)
  Burst type - Sequential / Interleave (programmable)
- Auto Precharge / All Bank Precharge controlled by A10
- Support concurrent Auto Precharge
- 4096 refresh cycles / 64ms (4 banks concurrent refresh)
- Auto Refresh and Self Refresh
- Row address A0-11 / Column address A0-9(x8) /A0-8(x16)
- SSTL_2 Interface
- Package 400-mil, 66-pin Thin Small Outline Package (TSOP II) with 0.65mm lead pitch

Pin Assignment (Top View) 66-pin TSOP

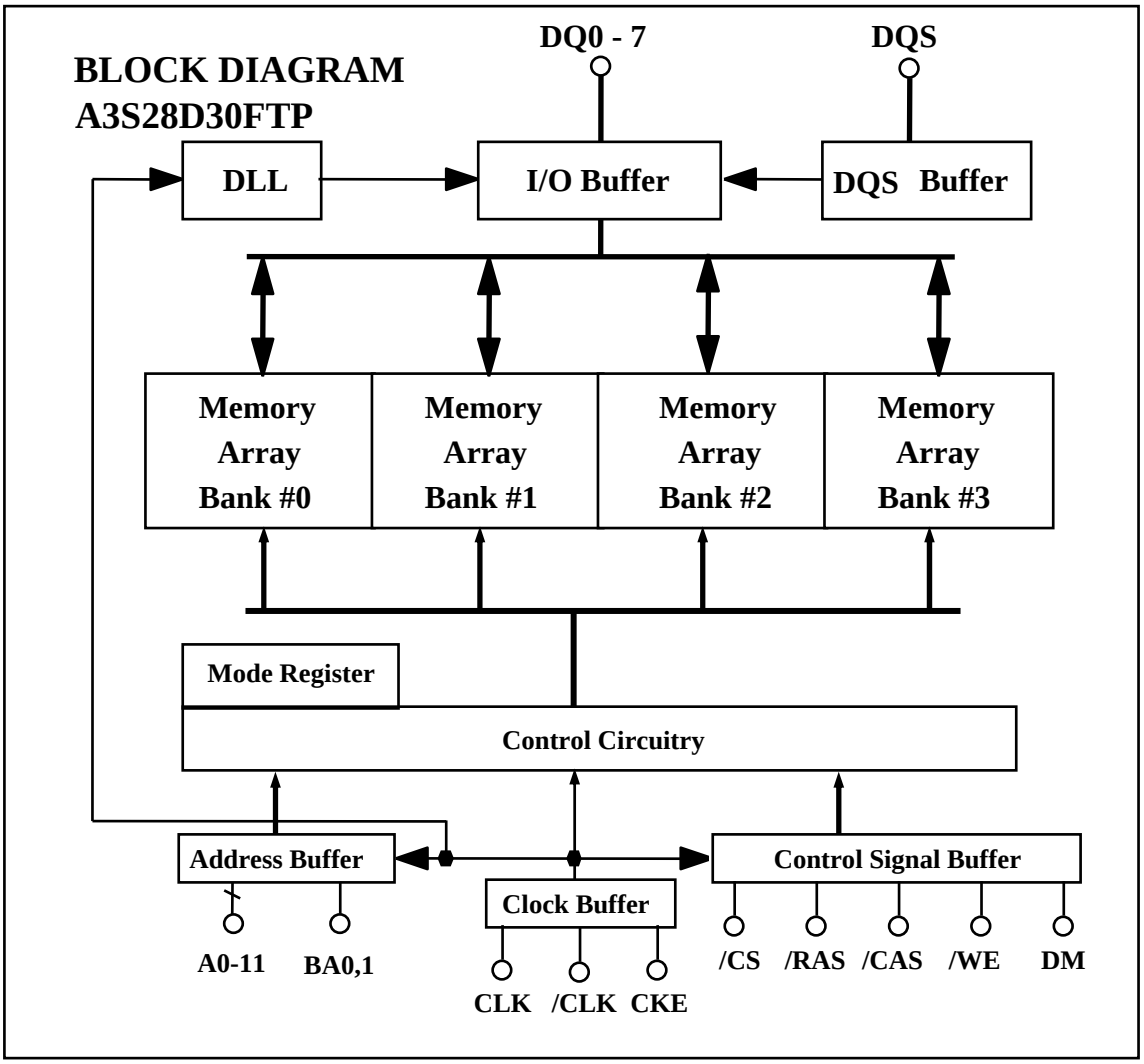


x16	x8			x16	x8
Vdd	Vdd	1	66	Vss	Vss
DQ0	DQ0	2	65	DQ15	DQ7
VddQ	VddQ	3	64	VssQ	VssQ
NC	DQ1	4	63	DQ14	NC
DQ1	DQ2	5	62	DQ13	DQ6
VssQ	VssQ	6	61	VddQ	VddQ
NC	DQ3	7	60	DQ12	NC
DQ2	DQ4	8	59	DQ11	DQ5
VddQ	VddQ	9	58	VssQ	VssQ
NC	DQ5	10	57	DQ10	NC
DQ3	DQ6	11	56	DQ9	DQ4
VssQ	VssQ	12	55	VddQ	VddQ
NC	DQ7	13	54	DQ8	NC
NC	NC	14	53	NC	NC
VddQ	VddQ	15	52	VssQ	VssQ
NC	LDQS	16	51	UDQS	DQS
NC	NC	17	50	NC	NC
Vdd	Vdd	18	49	VREF	VREF
NC	NC	19	48	Vss	Vss
NC	LDM	20	47	UDM	DM
/WE	/WE	21	46	/CLK	/CLK
/CAS	/CAS	22	45	CLK	CLK
/RAS	/RAS	23	44	CKE	CKE
/CS	/CS	24	43	NC	NC
NC	NC	25	42	NC	NC
BA0	BA0	26	41	A11	A11
BA1	BA1	27	40	A9	A9
A10/AP	A10/AP	28	39	A8	A8
A0	A0	29	38	A7	A7
A1	A1	30	37	A6	A6
A2	A2	31	36	A5	A5
A3	A3	32	35	A4	A4
Vdd	Vdd	33	34	Vss	Vss

CLK, /CLK	**: Master Clock**	**A0-11**	**: Address Input**
CKE	**: Clock Enable**	**BA0,1**	**: Bank Address Input**
/CS	**: Chip Select**	**Vdd**	**: Power Supply**
/RAS	**: Row Address Strobe**	**VddQ**	**: Power Supply for Output**
/CAS	**: Column Address Strobe**	**Vss**	**: Ground**
/WE	**: Write Enable**	**VssQ**	**: Ground for Output**
DQ0-15	**: Data I/O (x16)**	**VREF**	**: SSTL_2 reference voltage**
DQ0-7	**: Data I/O (x8)**		
UDM, LDM	**: Write Mask (x16)**		
DM	**: Write Mask (x8)**		
UDQS, LDQS	**: Data Strobe (x16)**		
DQS	**: Data Strobe (x8)**		

PIN FUNCTION

SYMBOL	TYPE	DESCRIPTION
CLK, /CLK	Input	Clock: CLK and /CLK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of /CLK. Output (read) data is referenced to the crossings of CLK and /CLK (both directions of crossing).
CKE	Input	Clock Enable: CKE controls Power Down and Self Refresh. Taking CKE LOW provides Precharge Power Down or Self Refresh (all banks idle), or Active Power Down (row active in any bank). Taking CKE HIGH provides Power Down exit or Self Refresh exit. After Self Refresh is started, CKE becomes asynchronous input. Power Down and Self Refresh is maintained as long as CKE is LOW.
/CS	Input	Chip Select: When /CS is HIGH, any command means No Operation.
/RAS, /CAS, /WE	Input	Combination of /RAS, /CAS, /WE defines basic commands.
A0-11	Input	A0-11 specify the Row / Column Address in conjunction with BA0,1. The Row Address is specified by A0-11. The Column Address is specified by A0-9(x8) and A0-8(x16). A10 is also used to indicate precharge option. When A10 is HIGH at a Read / Write command, an Auto Precharge is performed. When A10 is HIGH at a Precharge command, all banks are precharged.
BA0,1	Input	Bank Address: BA0,1 specifies one of four banks to which a command is applied. BA0,1 must be set with Active, Precharge, Read, Write commands.
DQ0-7 (x8), DQ0-15 (x16),	Input / Output	Data Input/Output: Data bus
DQS (x8) UDQS, LDQS (x16)	Input / Output	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS correspond to the data on DQ8-DQ15
DM (x8) UDM, LDM (x16)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-DQ7; UDM corresponds to the data on DQ8-DQ15.
Vdd, Vss	Power Supply	Power Supply for the memory array and peripheral circuitry.
VddQ, VssQ	Power Supply	VddQ and VssQ are supplied to DQ, DQS buffers.
VREF	Input	SSTL_2 reference voltage.

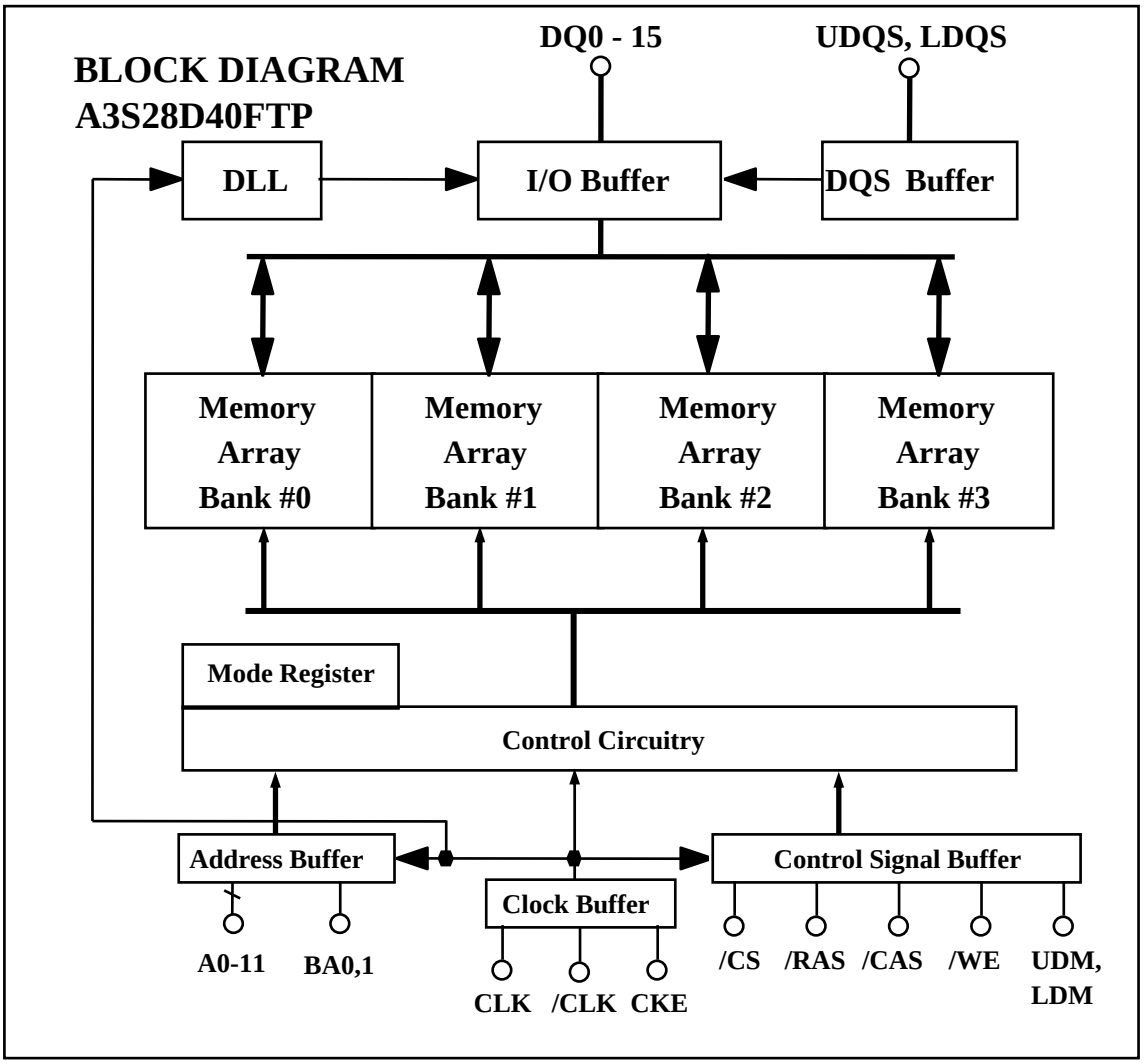


Type Designation Code

This rule is applied to only Synchronous DRAM family.

A 3 S 28 D 3 0 F TP –G4

- Speed Grade — G: Green part; 5: 200MHz @CL=3.0, 166MHz @CL=2.5, and 133MHz @CL=2.0; 5E: 200MHz @CL=3.0/2.5, and 133MHz @CL=2.0; 4: 250MHz @CL=3.0/4.0, 200MHz @CL2.5, and 133MHz @CL=2.0
- Package Type TP: TSOP(II)
- Process Generation
- Function Reserved for Future Use
- Organization 2^n 3: x8
- **DDR Synchronous DRAM**
- Density 28: 128M bits
- Interface S:SSTL_2
- Memory Style (DRAM)
- Zentel DRAM



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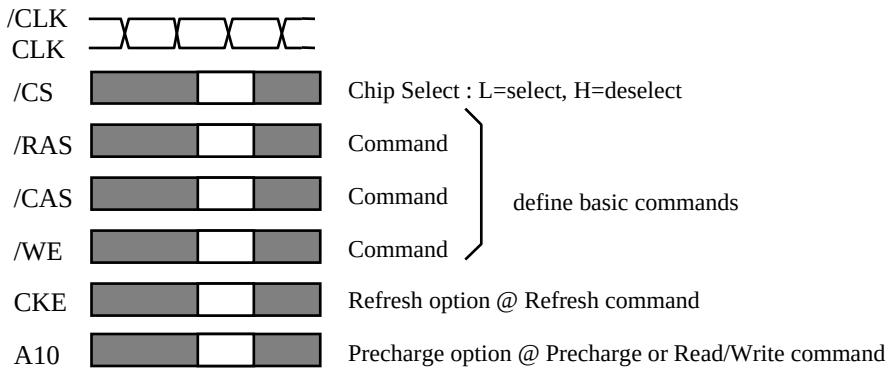
- Package Type TP: TSOP(II)
- Process Generation
- Function Reserved for Future Use
- Organization 2^n 4: x16
- **DDR Synchronous DRAM**
- Density 28: 128M bits
- Interface S:SSTL_2
- Memory Style (DRAM)
- Zentel DRAM

BASIC FUNCTIONS

The A3S28D30/40FTP provides basic functions, Active, Read / Write, Precharge, and Auto / Self Refresh, Mode Register Set, Burst Terminate. Each command is defined by control signals of /RAS, /CAS and /WE at CLK rising edge. In addition to 3 signals, /CS , CKE and A10 are used as chip select, refresh option, and precharge option, respectively. To know the detailed definition of commands, please see the command truth table.



Deselect (DESEL) [/CS = H, /RAS = X, /CAS = X, /WE = X]

DESEL command prevents new commands from being executed. Operations already in progress are not affected.

No Operation (NOP) [/CS = L, /RAS = H, /CAS = H, /WE = H]

NOP command prevents unwanted commands from being registered. NOP command is effectively the same as DESEL command. Operations already in progress are not affected.

Mode Register Set (MRS) [/CS = L, /RAS = L, /CAS = L, /WE = L]

MRS command loads the mode registers via inputs BA0,1, and A0-A11. The MRS command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.

Active (ACT) [/CS = L, /RAS = L, /CAS = H, /WE = H]

ACT command activates a row in an idle bank indicated by BA.

Read (READ) [/CS = L, /RAS = H, /CAS = L, /WE = H]

READ command starts burst read from the active bank indicated by BA. First output data appears after /CAS latency. When A10 = H at this command, the bank is deactivated after the burst read (Read with Auto Precharge, **READA**).

Write (WRITE) [/CS = L, /RAS = H, /CAS = L, /WE = L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 = H at this command, the bank is deactivated after the burst write (Write with Auto Precharge, **WRITEA**).

Burst Terminate (TERM) [/CS = L, /RAS = H, /CAS = H, /WE = L]

TERM command is used to truncate read bursts (with auto precharge disabled).
The most recently registered READ command prior to the TERM command will be truncated.

Precharge (PRE) [/CS = L, /RAS = L, /CAS = H, /WE = L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read / write operation. When A10 = H at this command, all banks are deactivated (Precharge All Banks, **PREA**). PRE command is treated as a NOP command if there is no open row in that bank, or if the previously open row is already in the process of precharging.

Auto Refresh (REFA) [/CS = L, /RAS = L, /CAS = L, /WE = H, CKE =H]

REFA command starts Auto Refresh cycle. Refresh addresses including bank addresses are generated internally. After REFA command, the banks are precharged automatically. Only DESEL or NOP command is allowed within a period of tRFC from REFA command. The DDR SDRAM requires Auto Refresh cycles at an average periodic interval of tREFI (maximum), with some flexibility that a maximum of eight Auto Refresh commands can be posted and the maximum absolute interval between any Auto Refresh command and the next Auto Refresh command is 8*tREFI.

Self Refresh (REFS) [/CS = L, /RAS = L, /CAS = L, /WE = H, CKE =L]

REFS command starts Self Refresh. When in the Self Refresh mode, the DDR SDRAM retains data without external clocking. The DLL is automatically disabled upon entering Self Refresh, and is automatically enabled upon exiting Self Refresh. Input signals except CKE are “Don’t Care” during Self Refresh. Since CKE is an SSTL_2 input, VREF must be maintained during Self Refresh.

COMMAND TRUTH TABLE

COMMAND	MNEMONIC	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	BA0,1	A10 /AP	A0-9, 11	note
Deselect	DESEL	H	X	H	X	X	X	X	X	X	
No Operation	NOP	H	X	L	H	H	H	X	X	X	
Row Address Entry & Bank Active	ACT	H	H	L	L	H	H	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	V	L	X	
Precharge All Banks	PREA	H	H	L	L	H	L	X	H	X	
Column Address Entry & Write	WRITE	H	H	L	H	L	L	V	L	V	
Column Address Entry & Write with Auto Precharge	WRITEA	H	H	L	H	L	L	V	H	V	
Column Address Entry & Read	READ	H	H	L	H	L	H	V	L	V	
Column Address Entry & Read with Auto Precharge	READA	H	H	L	H	L	H	V	H	V	
Auto Refresh	REFA	H	H	L	L	L	H	X	X	X	
Self Refresh Entry	REFS	H	L	L	L	L	H	X	X	X	
Self Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X	
		L	H	L	H	H	H	X	X	X	
Burst Terminate	TERM	H	H	L	H	H	L	X	X	X	1
Mode Register Set	MRS	H	H	L	L	L	L	L	L	V	2

H=HIGH Level, L=LOW Level, V=Valid, X=Don't Care, n=CLK cycle number

NOTE:

1. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts.
2. BA0-BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-A11 provide the op-code to be written to the selected Mode Register.

FUNCTION TRUTH TABLE

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
IDLE	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	Bank Active, Latch RA	
	L	L	H	L	BA, A10	PRE / PREA	NOP	4
	L	L	L	H	X	REFA	Auto-Refresh	5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set	5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	H	BA, CA, A10	READ / READA	Begin Read, Latch CA, Determine Auto-Precharge	
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto-Precharge	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Precharge / Precharge All	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
READ(Auto Precharge Disabled)	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	Terminate Burst	
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge	3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
WRITE(Auto Precharge Disabled)	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin Read, Determine Auto-Precharge	3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge	3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
READ with Auto Precharge	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ / READA	Support Concurrent Auto-Precharge	6
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Support Concurrent Auto-Precharge	6
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2, 6
	L	L	H	L	BA, A10	PRE / PREA	Precharge / ILLEGAL	2, 6
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
WRITE with Auto Precharge	H	X	X	X	X	DESEL	NOP (Continue Burst to END)	
	L	H	H	H	X	NOP	NOP (Continue Burst to END)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ / READA	Support Concurrent Auto-Precharge	6
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Support Concurrent Auto-Precharge	6
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL	2, 6
	L	L	H	L	BA, A10	PRE / PREA	Precharge / ILLEGAL	2, 6
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
PRE-CHARGING	H	X	X	X	X	DESEL	NOP (Idle after tRP)	
	L	H	H	H	X	NOP	NOP (Idle after tRP)	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	NOP (Idle after tRP)	4
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP (Row Active after tRCD)	
	L	H	H	H	X	NOP	NOP (Row Active after tRCD)	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
WRITE RE-COVERING	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	BA	TERM	ILLEGAL	2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	2
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
REFRESHING	H	X	X	X	X	DESEL	NOP (Idle after tRC)	
	L	H	H	H	X	NOP	NOP (Idle after tRC)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Row Active after tRSC)	
	L	H	H	H	X	NOP	NOP (Row Active after tRSC)	
	L	H	H	L	BA	TERM	ILLEGAL	
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

ABBREVIATIONS:

H=HIGH Level, L=LOW Level, X=Don't Care

BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No Operation

NOTES:

1. All entries assume that CKE was HIGH during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.
6. Concurrent Auto Precharge supported;
   A Read with Auto Precharge or a Write with Auto Precharge may be followed by any command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply (e.g., contention between read data and write data must be avoided). The minimum delay from a Read with Auto Precharge or a Write with Auto Precharge to a command to a different bank is summarized below.

From command	To command (different bank)	Minimum delay	Units
Write w/AP	Read or Read w/AP	1 + (BL/2) + tWTR	tCK
	Write or Write w/AP	BL/2	tCK
	Precharge or Active	1	tCK
Read w/AP	Read or Read w/AP	BL/2	tCK
	Write or Write w/AP	CL(round up) + (BL/2)	tCK
	Precharge or Active	1	tCK

7. ILLEGAL = Device operation and/or data-integrity are not guaranteed.

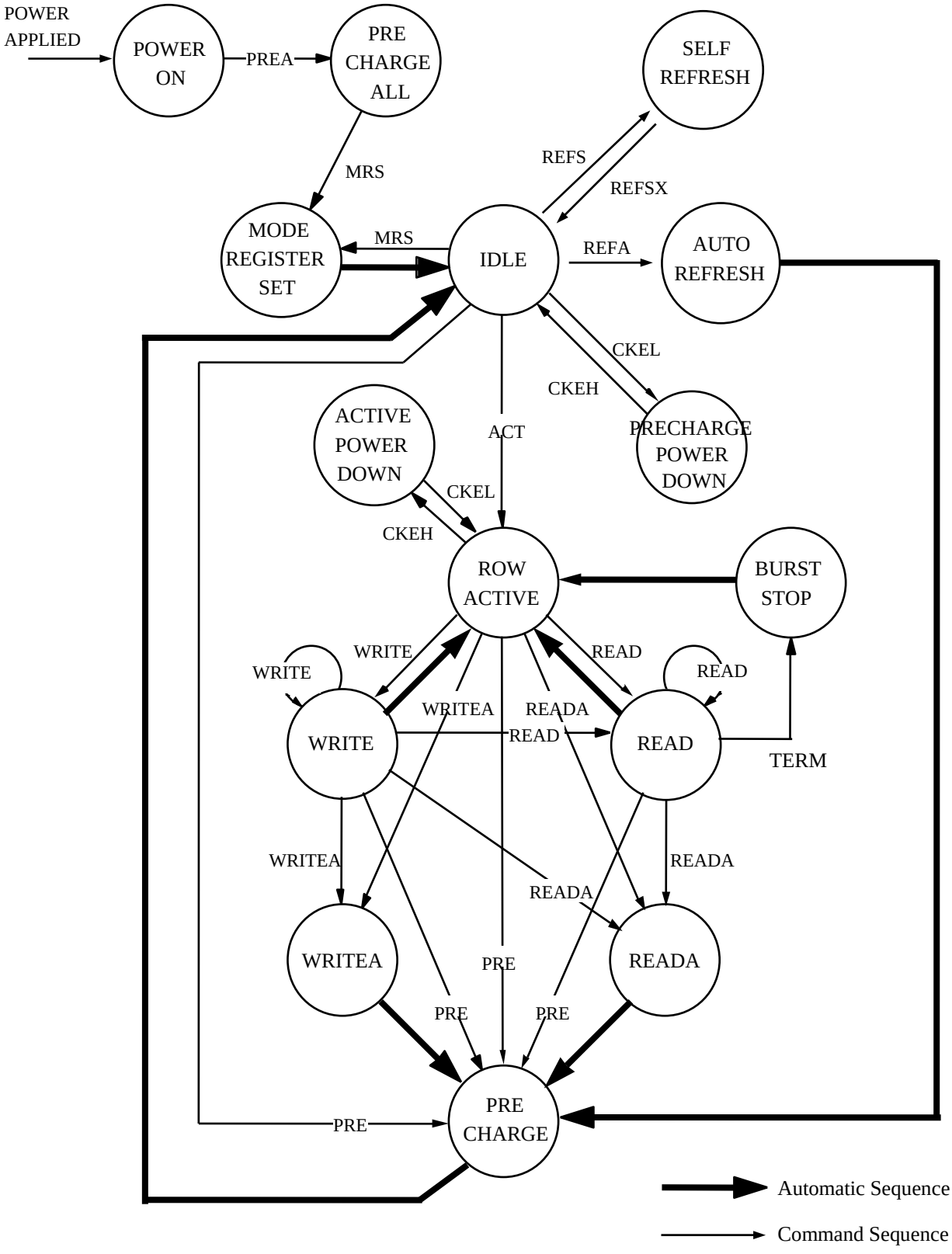
FUNCTION TRUTH TABLE for CKE

CKE n-1	CKE n	Current State	Command n	Action n	Notes
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	7
L	H	Power Down	Deselect or Nop	Exit Power Down	
L	H	Self Refresh	Deselect or Nop	Exit Self Refresh	5, 7
H	L	All Banks Idle	Deselect or Nop	Precharge Power Down Entry	
H	L	Bank(s) Active	Deselect or Nop	Active Power Down Entry	
H	L	All Banks Idle	Auto Refresh	Self Refresh Entry	
H	H		See Function Truth Table		

NOTES:

1. CKE n is the logic state of CKE at clock edge n; CKE n-1 was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
3. Command n is the command registered at clock edge n, and Action n is a result of Command n.
4. All states and sequences not shown are illegal or reserved.
5. DESEL or NOP commands should be issued on any clock edges occurring during the tXSNR or tXSRD period. A minimum of 200 clock cycles is needed before applying any executable command, for the DLL to lock.
6. Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
7. VREF must be maintained during Self Refresh operation.

SIMPLIFIED STATE DIAGRAM



POWER UP & INITIALIZATION SEQUENCE

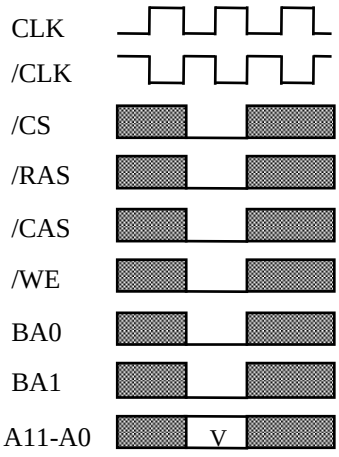
DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

1. Apply VDD before or with VDDQ such that VDDQ < VDD+0.3V.
2. Apply VDDQ before or with VTT & VREF such that VTT < VDDQ+0.3V & VREF < VDDQ+0.3V.
3. During power up, maintain an LVCMOS LOW level on CKE to keep DQ & DQS in the High-Z state.
4. After all power supply and reference voltages are stable, and CLK are stable, the DDR SDRAM requires a 200us delay prior to applying an executable command.
5. CKE should be brought HIGH while keeping NOP or DESEL command.
6. Issue a PRECHARGE ALL command.
7. Issue an MRS command for the Extended Mode Register to enable the DLL.
8. Issue an MRS command for the Mode Register to reset the DLL and to program the operating parameters.
9. Maintain stable condition for 200 cycles for the DLL to lock.
10. Issue a PRECHARGE ALL command.
11. Once in the idle state, issue two AUTO REFRESH commands.
12. An MRS command for the Mode Register for programming the operating parameters with DLL reset bit deactivated may be followed.

Following these cycles, the DDR SDRAM is idle and ready for normal operation.

MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register. The mode register stores these data until the next MRS command for the mode register, which may be issued when all banks are in idle state. The DLL is reset by setting A8 of the mode register to one with A6-A0 set to the desired values. After tMRD from an MRS command for the mode register, the DDR SDRAM is ready for a new command other than READ or READA. READ or READA command can be issued after 200 stable clock cycles from the MRS command with DLL reset.



BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	DR	0	LTMODE			BT	BL		

	CL	/CAS Latency
Latency Mode	0 0 0	R
	0 0 1	R
	0 1 0	2
	0 1 1	3
	1 0 0	4
	1 0 1	R
	1 1 0	2.5
	1 1 1	R

	BL	BT=0	BT=1
Burst Length	0 0 0	R	R
	0 0 1	2	2
	0 1 0	4	4
	0 1 1	8	8
	1 0 0	R	R
	1 0 1	R	R
	1 1 0	R	R
	1 1 1	R	R

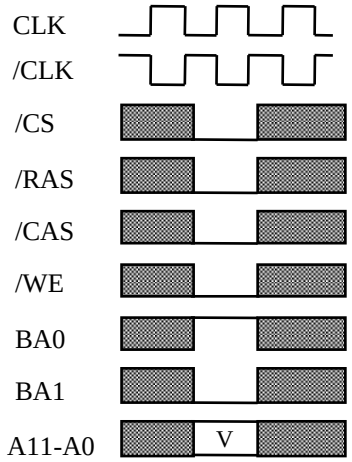
DLL Reset	0	NO
	1	YES

Burst Type	0	Sequential
	1	Interleaved

R: Reserved for Future Use

EXTENDED MODE REGISTER

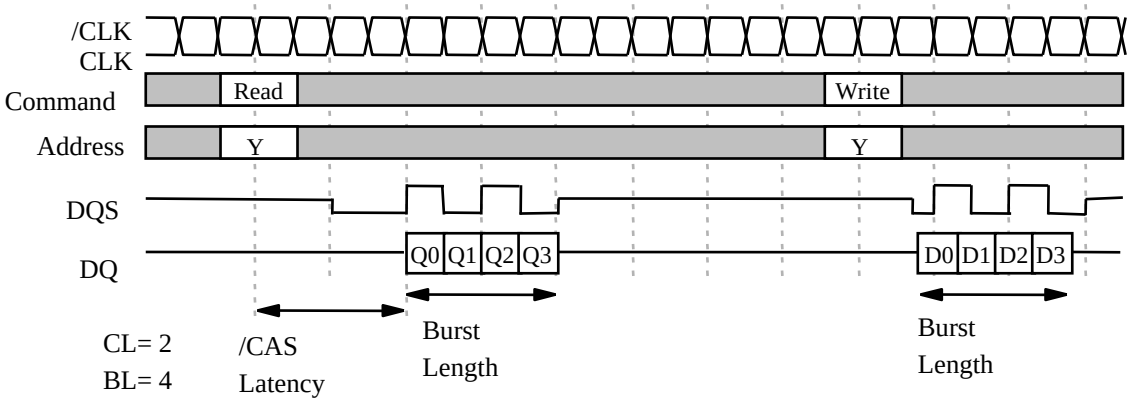
DLL enable/disable mode and drive strength for DQ/DQS output buffers can be programmed by setting the extended mode register. The extended mode register stores these data until the next MRS command for the extended mode register, which may be issued when all banks are in idle state. After tMRD from an MRS command for the extended mode register, the DDR SDRAM is ready for a new command.



BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	0	0	0	0	0	0	DS	DD

DLL Disable	0	DLL Enable
	1	DLL Disable

Drive Strength	0	Normal
	1	Weak



Initial Address			BL	Column Addressing															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vdd	Supply Voltage	with respect to Vss	-1 ~ 3.6	V
VddQ	I/O Supply Voltage	with respect to VssQ	-1 ~ 3.6	V
VI	Voltage on Inputs	with respect to Vss	-1 ~ 3.6	V
VO	Voltage on I/O Pins	with respect to VssQ	-0.5 ~ VddQ+0.5	V
IO	Output Current		50	mA
Pd	Power Dissipation	Ta = 25 °C	1	W
Ta	Operating Temperature (ambient)		0 ~ 70	°C
Tstg	Storage Temperature		-55 ~ 150	°C

DC OPERATING CONDITIONS

(Ta=0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit	Notes
		Min.	Typ.	Max.		
Vdd	Supply Voltage	2.3	2.5	2.7	V	
VddQ	I/O Supply Voltage	2.3	2.5	2.7	V	
VREF	I/O Reference Volatage	0.49*VddQ	0.5*VddQ	0.51*VddQ	V	
VTT	I/O Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	
VIH(DC)	Input High Voltage	VREF+0.15		Vdd+0.3	V	
VIL(DC)	Input Low Voltage	-0.3		VREF-0.15	V	
VIN(DC)	Input Voltage Level, CLK and /CLK inputs	-0.3		VddQ+0.3	V	
VID(DC)	Input Differential Voltage, CLK and /CLK inputs	0.36		VddQ+0.6	V	
IL	Input Leakage Current, Any input 0V≤VIN≤VDD (All other pins not under test = 0V)	-2	—	2	uA	
IOZ	Output Leakage Current DQs are disabled ; 0V≤Vout≤VddQ	-5	—	5	uA	
IOH	Output High Current (VOUT=1.95V)	-16.2	—	—	mA	
IOL	Output Low Current (VOUT=0.35V)	16.2	—	—	mA	

AC OPERATING CONDITIONS

(Ta=0 ~ 70°C, Vdd = VddQ = 2.5V ± 0.2V, Vss = VssQ = 0V, unless otherwise noted)

Symbol	Parameter	Limits			Unit	Notes
		Min.	Typ.	Max.		
VIH(AC)	Input High Voltage	VREF+0.31			V	
VIL(AC)	Input Low Voltage			VREF-0.31	V	
VID(AC)	Input Differential Voltage, CLK and /CLK inputs	0.7		VddQ+0.6	V	
VIX(AC)	Input Crossing Point Voltage, CLK and /CLK inputs	0.5*VddQ-0.2	0.5*VddQ	0.5*VddQ+0.2	V	

CAPACITANCE

(Ta=0 ~ 70°C, Vdd = VddQ = 2.5V ± 0.2V, Vss = VssQ = 0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits		Delta Cap.(Max.)	Unit	Notes
			Min.	Max.			
CI1	Input Capacitance, CLK, /CLK	f=100MHz, Ta=25°C	2.5	3.5	0.25	pF	11
CI2	Input Capacitance, all other input-only pins	Vout(DC)=VddQ/2	2.5	3.5	1.0	pF	11
CI/O	I/O Capacitance, DQ, DQS, DM	Vout p-p=0.2V	4.0	5.0	1.0	pF	11

AVERAGE SUPPLY CURRENT from Vdd

(Ta=0 ~ 70°C, Vdd = VddQ = 2.5V ± 0.2V, Vss = VssQ = 0V, Output Open, unless otherwise noted)

Symbol	Parameter/Test Conditions	Limits(Max.)			Unit	Notes
		-4	-5E	-5		
IDD0	OPERATING CURRENT FOR ONE BANK ACTIVE-PRECHARGE: One bank active-precharge; tRC = tRC(min); tCK = tCK(min); DQ, DQS and DM inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles; /CS = HIGH between valid commands	140	135	135	mA	
IDD1	OPERATING CURRENTFOR ONE BANK OPERATION: One bank active-read-precharge; Burst Length = 4; tRC = tRC(min); tCK = tCK(min); IOUT= 0mA; Address and control inputs changing once per clock cycle; /CS = HIGH between valid commands; 50% of data changing on every transfer	155	150	150		
IDD2P	PRECHARGE POWER DOWN STANDBY CURRENT: All banks idle; Power Down mode; CKE ≤ VIL(max); tCK = tCK(min); VIN = VREF for DQ, DQS, and DM	30	30	30		
IDD2F	PRECHARGE FLOATING STANDBY CURRENT: /CS ≥ VIH(min); All banks idle; CKE ≥ VIH(min); tCK = tCK(min); Address and other control inputs changing once per clock cycle; VIN = VREF for DQ, DQS, and DM	65	65	65		
IDD2Q	PRECHARGE QUIET STANDBY CURRENT: /CS ≥ VIH(min); All banks idle; CKE ≥ VIH(min); tCK = tCK(min); Address and other control inputs stable at ≥ VIH(min) or ≤ VIL(max); VIN = VREF for DQ, DQS, and DM	60	60	60		
IDD3P	ACTIVE POWER DOWN STANDBY CURRENT: One bank active; Power Down mode; CKE ≤ VIL(max); tCK = tCK(min); VIN = VREF for DQ, DQS, and DM	40	40	40		
IDD3N	ACTIVE STANDBY CURRENT: /CS ≥ VIH(min); CKE ≥ VIH(min); One bank active; tRC = tRAS(max); tCK = tCK(min); DQ, DQS and DM inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	115	115	115		
IDD4R	OPERATING CURRENT FOR BURST READ: Burst Length = 2; Read; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK = tCK(min); 50% of data changing on every transfer; IOUT = 0 mA	195	180	180		
IDD4W	OPERATING CURRENTFOR BURST WRITE: Burst Length = 2; Write ; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK = tCK(min); DQ, DQS, and DM inputs changing twice per clock cycle; 50% of input data changing at every transfer	180	165	165		
IDD5	AUTO REFRESH CURRENT: tRC = tRFC(min)	155	150	150		
IDD6	SELF REFRESH CURRENT: CKE ≤ 0.2V, tCK = tCK(min)	5	5	5		
IDD7	OPERATING CURRENT FOR FOUR BANK OPERATION: four bank interleaving with Burst Length = 4, refer to note.22 for detailed test condition	295	295	295		22

AC TIMING REQUIREMENTS

(Ta=0 ~ 70°C, unless otherwise noted)

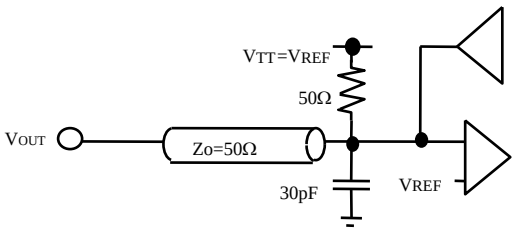
Symbol	AC Characteristics Parameter		-4		-5E		-5		Unit	Notes
			Min.	Max	Min.	Max	Min.	Max		
tAC	DQ output access time from CLK//CLK		-0.70	+0.70	-0.70	+0.70	-0.70	+0.70	ns	
tDQSCK	DQS output access time from CLK//CLK		-0.6	+0.6	-0.6	+0.6	-0.6	+0.6	ns	
tCH	CLK HIGH level width		0.45	0.55	0.45	0.55	0.45	0.55	tCK	
tCL	CLK LOW level width		0.45	0.55	0.45	0.55	0.45	0.55	tCK	
tCK	CLK cycle time	CL=4.0	4	12	-	-	-	-	ns	
		CL=3.0	4	12	5	12	5	12	ns	
		CL=2.5	5	12	5	12	6	12	ns	
		CL=2.0	7.5	12	7.5	12	7.5	12	ns	
tDS	Input setup time (DQ,DM)		0.4		0.4		0.4		ns	
tDH	Input hold time(DQ,DM)		0.4		0.4		0.4		ns	
tIPW	Control & address input pulse width (for each input)		2.2		2.2		2.2		ns	
tDIPW	DQ and DM input pulse width (for each input)		1.75		1.75		1.75		ns	
tHZ	Data-out high impedance time from CLK//CLK			+0.70		+0.70		+0.70	ns	14
tLZ	Data-out low impedance time from CLK//CLK		-0.70	+0.70	-0.70	+0.70	-0.70	+0.70	ns	14
tDQSQ	DQ valid data delay time from DQS			0.40		0.40		0.40	ns	
tHP	Clock half period		tCLmin or tCHmin		tCLmin or tCHmin		tCLmin or tCHmin		ns	20
tQH	DQ output hold time from DQS (per access)		tHP-tQHS		tHP-tQHS		tHP-tQHS		ns	
tQHS	Data hold skew factor (for DQS & associated DQ signals)			0.50		0.50		0.50	ns	
tDQSS	Write command to first DQS latching transition		0.72	1.15	0.72	1.25	0.72	1.25	tCK	
tDQSH	DQS input HIGH level width		0.35		0.35		0.35		tCK	
tDQSL	DQS input LOW level width		0.35		0.35		0.35		tCK	
tDSS	DQS falling edge to CLK setup time		0.25		0.2		0.2		tCK	
tDSH	DQS falling edge hold time from CLK		0.2		0.2		0.2		tCK	
tMRD	Mode Register Set command cycle time		2		2		2		tCK	
tWPRES	Write preamble setup time		0		0		0		ns	16
tWPST	Write postamble		0.4	0.6	0.4	0.6	0.4	0.6	tCK	15
tWPRE	Write preamble		max(0.25* tCK, 1.5ns)		max(0.25* tCK, 1.5ns)		max(0.25* tCK, 1.5ns)		ns	
tIS	Input Setup time (address and control)		0.6		0.6		0.6		ns	19
tIH	Input Hold time (address and control)		0.6		0.6		0.6		ns	19
tRPST	Read postamble		0.4	0.6	0.4	0.6	0.4	0.6	tCK	
tRPRE	Read preamble		0.9	1.1	0.9	1.1	0.9	1.1	tCK	

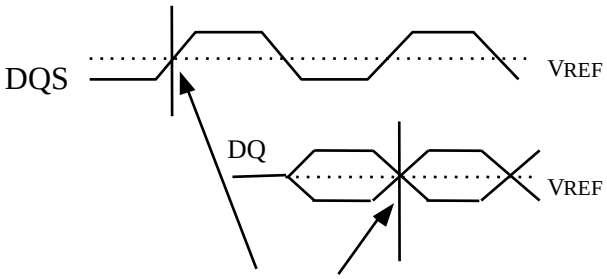
AC TIMING REQUIREMENTS(Continues)

(Ta=0 ~ 70°C, unless otherwise noted)

Symbol	AC Characteristics Parameter	-4		-5E		-5		Unit	Notes
		Min.	Max	Min.	Max	Min.	Max		
tRAS	Row active time	40	120,000	40	120,000	40	120,000	ns	
tRC	Row cycle time(operation)	55		55		55		ns	
tRFC	Auto Refresh to Active/Auto Refresh command period	70		70		70		ns	
tRCD	Row to column delay	15		15		15		ns	
tRP	Row precharge time	15		15		15		ns	
tRRD	Act to Act delay time	10		10		10		ns	
tWR	Write recovery time	15		15		15		ns	
tDAL	Auto Precharge write recovery + precharge time							tCK	21
tWTR	Internal Write to Read command delay	2		2		2		tCK	
tXSNR	Exit Self Refresh to non-Read command	75		75		75		ns	
tXSRD	Exit Self Refresh to Read command	200		200		200		tCK	
tXPNR	Exit Power Down to command	1		1		1		tCK	
tXPRD	Exit Power Down to Read command	1		1		1		tCK	18
tREFI	Average periodic refresh interval		15.6		15.6		15.6	µs	17

Output Load Condition

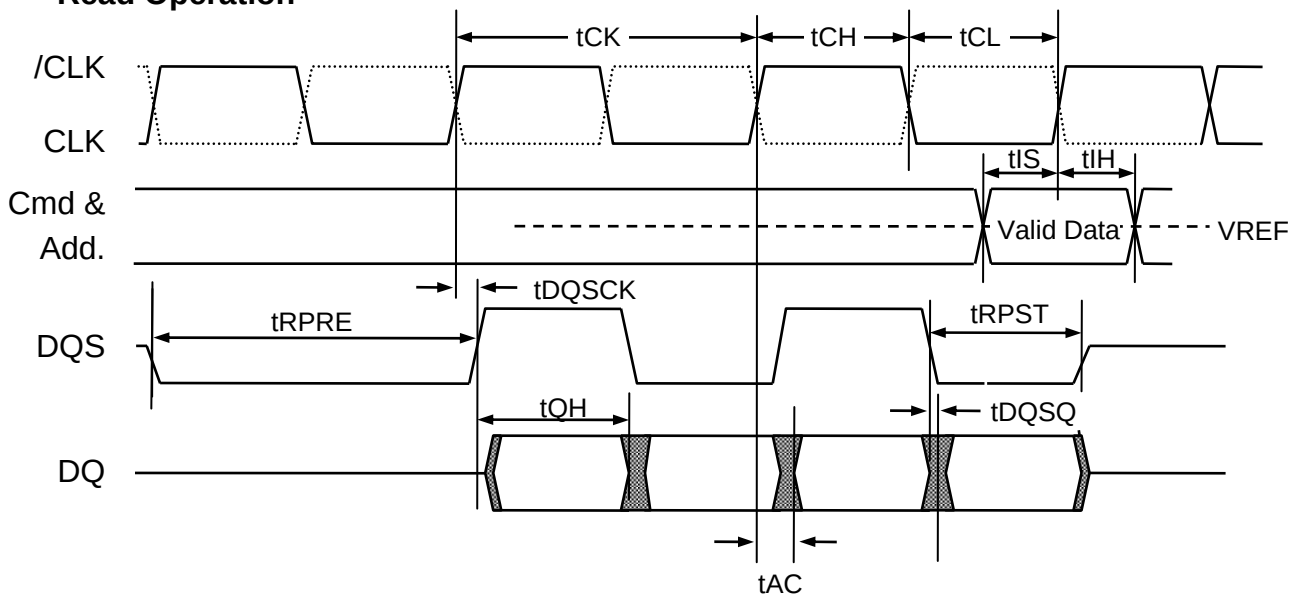




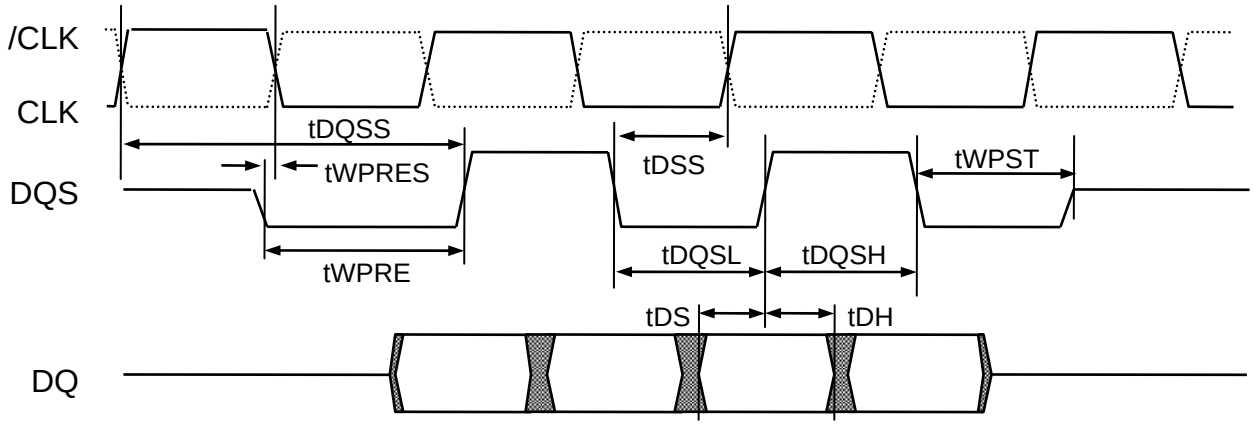
Output Timing Measurement Reference Point

Notes
1. All voltages referenced to Vss.
2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CLK//CLK), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between VIL(AC) and VIH(AC).
4. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
5. VREF is expected to be equal to 0.5*VddQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed $\pm$2% of the DC value.
6. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.
7. VID is the magnitude of the difference between the input level on CLK and the input level on /CLK.
8. The value of VIX is expected to equal 0.5*VddQ of the transmitting device and must track variations in the DC level of the same.
9. Enables on-chip refresh and address counters.
10. IDD specifications are tested after the device is properly initialized.
11. This parameter is sampled. VddQ = 2.5V$\pm$0.2V, Vdd = 2.5V $\pm$ 0.2V , f = 100 MHz, Ta = 25^{o}C, VOUT(DC) = VddQ/2, VOUT(PEAK TO PEAK) = 0.2V. DM inputs are grouped with I/O pins - reflecting the fact that they are matched in loading (to facilitate trace matching at the board level).
12. The CLK//CLK input reference level (for timing referenced to CLK//CLK) is the point at which CLK and /CLK cross; the input reference level for signals other than CLK//CLK, is VREF.
13. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE$\leq$ 0.3VddQ is recognized as LOW.
14. t HZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ), or begins driving (LZ).
15. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
16. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CLK edge. A valid transition is defined as monotonic, and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
17. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
18. tXPRD should be 200 tCLK in the condition of the unstable CLK operation during the Power Down mode.
19. For command/address and CLK & /CLK slew rate > 1.0V/ns.
20. Min (tCL,tCH) refers to the smaller of the actual clock LOW time and the actual clock HIGH time as provided to the
device.
21. tDALminimum = (tWR/tCK) + (tRP/tCK).
For each of the terms above, if not already an integer, round to the next highest integer.
22. Operating current for four bank operation: Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on Deselect edge are not changing. IOUT = 0mA.
Test pattern for -5E, -5 (200MHz, CL = 3, tCK = 5ns, BL = 4, tRRD = 2*tCK, tRCD = 3*tCK, tRC = 11*tCK);
Setup; A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 N
Read; A0 N A1 RA0 A2 RA1 A3 RA2 N RA3 N
Test pattern for -4 (250MHz, CL = 3, tCK = 4ns, BL = 4, tRRD = 3*tCK, tRCD = 4*tCK, tRC = 14*tCK);
Setup; A0 N N A1 RA0 N A2 RA1 N A3 RA2 N N RA3
Read; A0 N N A1 RA0 N A2 RA1 N A3 RA2 N N RA3
Repeat the same timing with random address changing, 50% of data changing at every transfer.

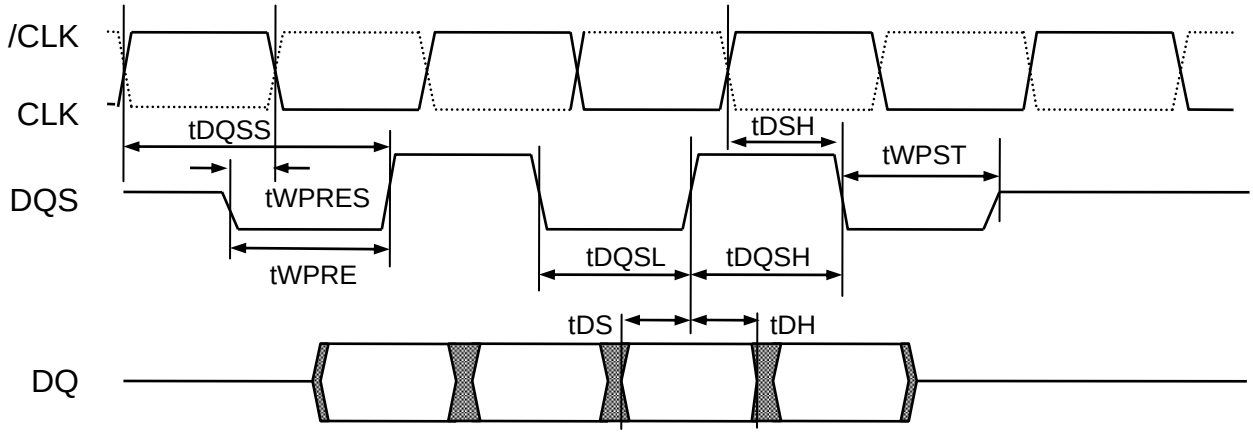
Read Operation



Write Operation / tDQSS=max.



Write Operation / tDQSS=min.



OPERATIONAL DESCRIPTION

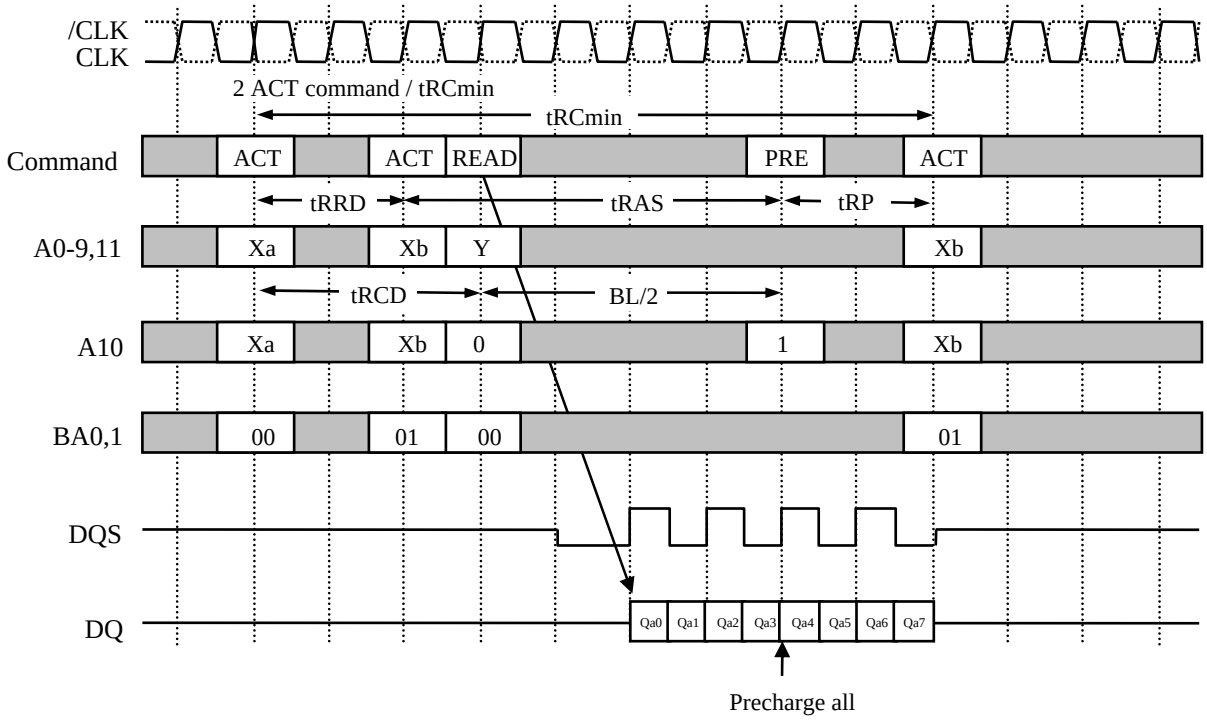
BANK ACTIVATE

The DDR SDRAM has four independent banks. Each bank is activated by the ACT command with the bank addresses (BA0,1). A row is indicated by the row address A0-11. The minimum activation interval between one bank and the other bank is tRRD.

PRECHARGE

The PRE command deactivates the bank indicated by BA0,1. When multiple banks are active, the precharge all command (PREA,PRE+A10=H) is available to deactivate them at the same time. After tRP from the precharge, an ACT command to the same bank can be issued.

Bank Activation and Precharge All (BL=8, CL=2)

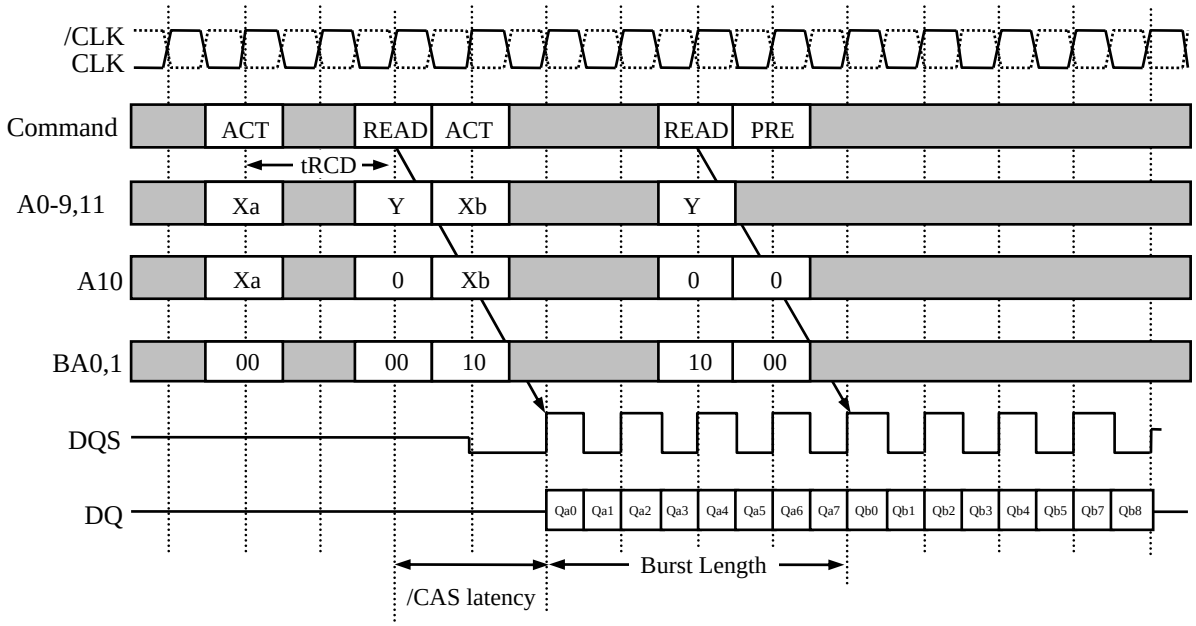


A precharge command can be issued at BL/2 from a read command without data loss.

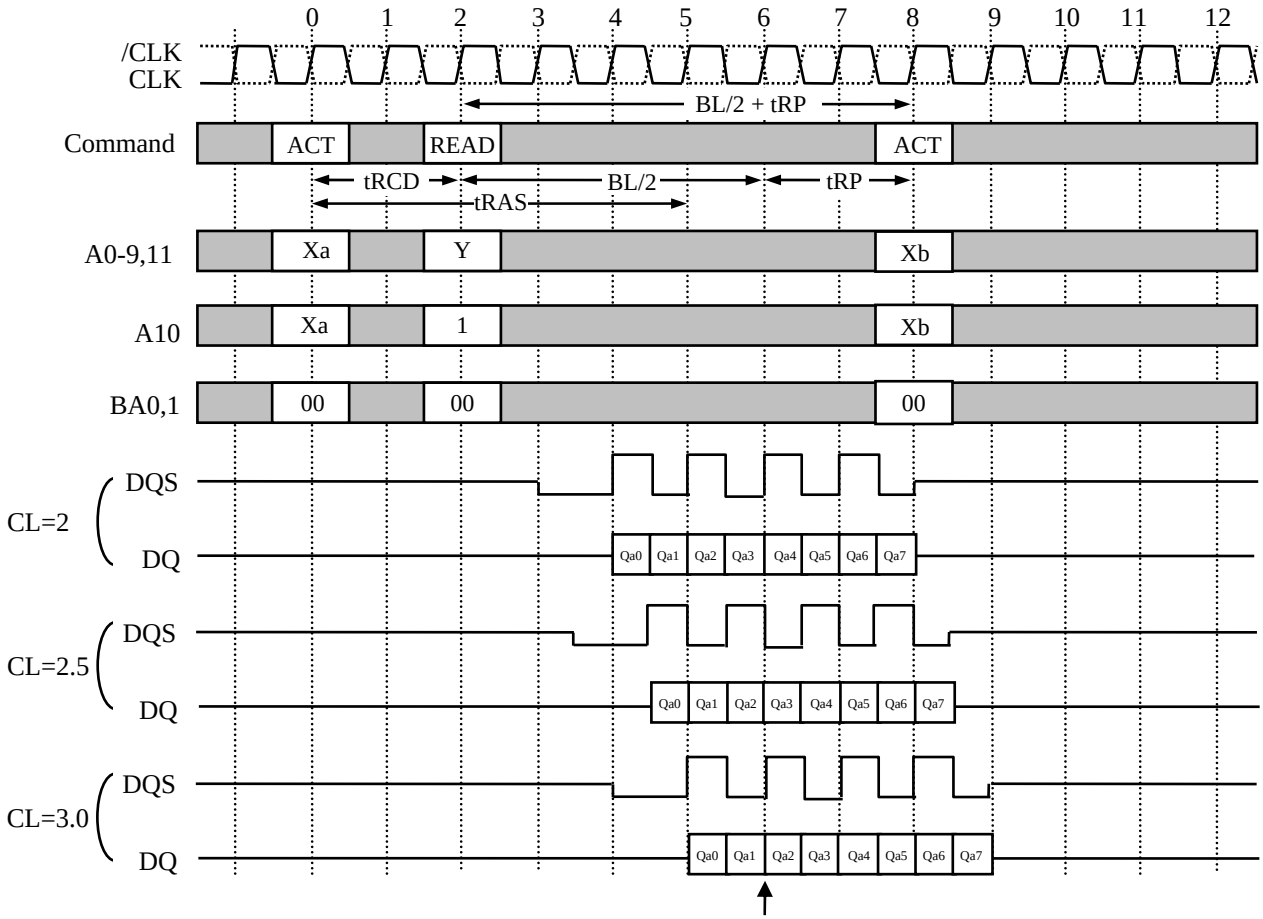
READ

After tRCD from the bank activation, a READ command can be issued. 1st Output data is available after the /CAS Latency from the READ, followed by (BL-1) consecutive data when the Burst Length is BL. The start address is specified by A0-9(x8)/A0-8(x16), and the address sequence of burst data is defined by the Burst Type. A READ command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous output data by interleaving the multiple banks. When A10 is HIGH at a READ command, the auto-precharge (READA) is performed. The internal precharge starts at the later time of either BL/2 after READA or tRAS after ACT. The next ACT command can be issued after tRP from the internal precharge.

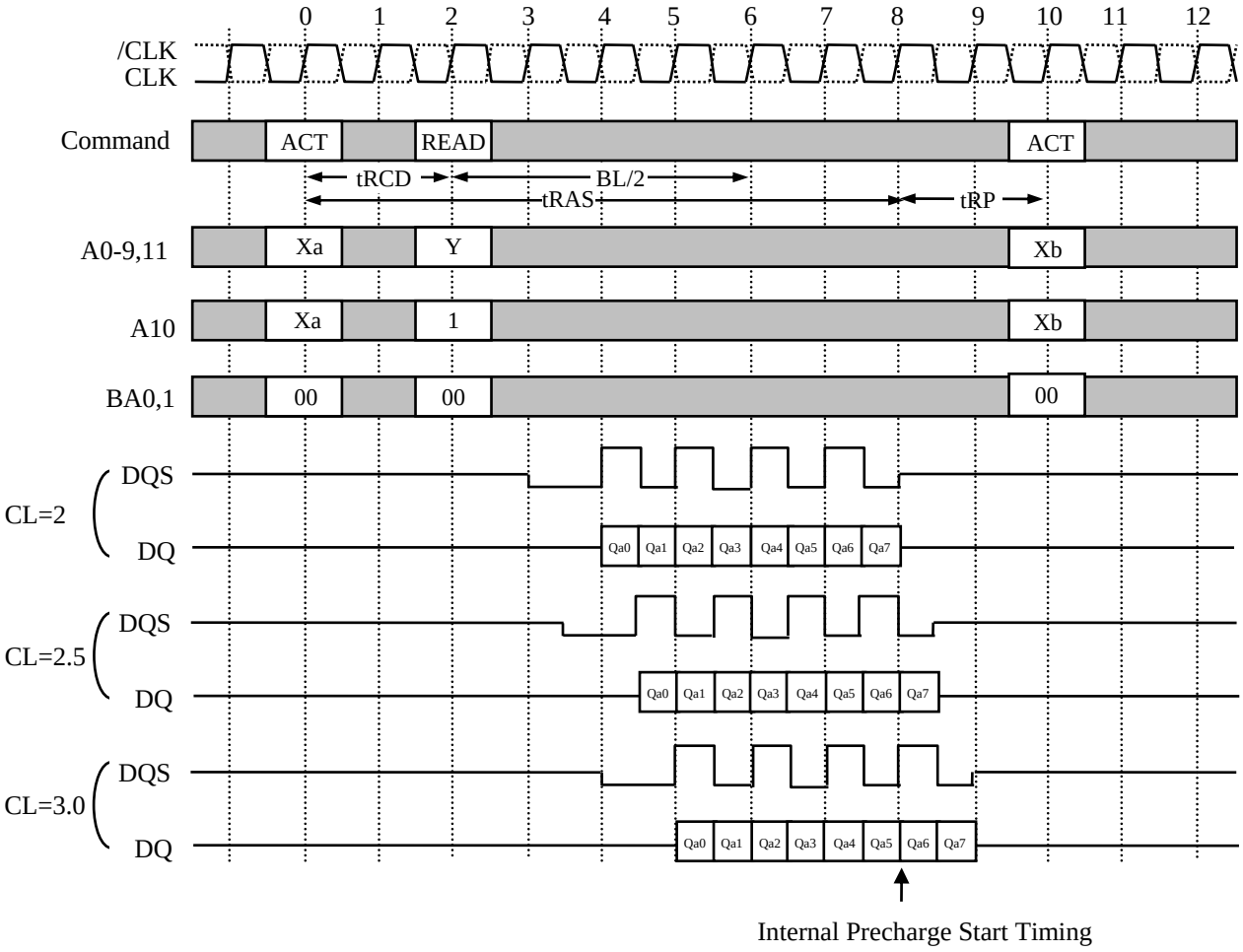
Multi Bank Interleaving READ (BL=8, CL=2)



READ with Auto-Precharge (BL=8, CL=2,2.5,3.0) (BL/2 determinant case)



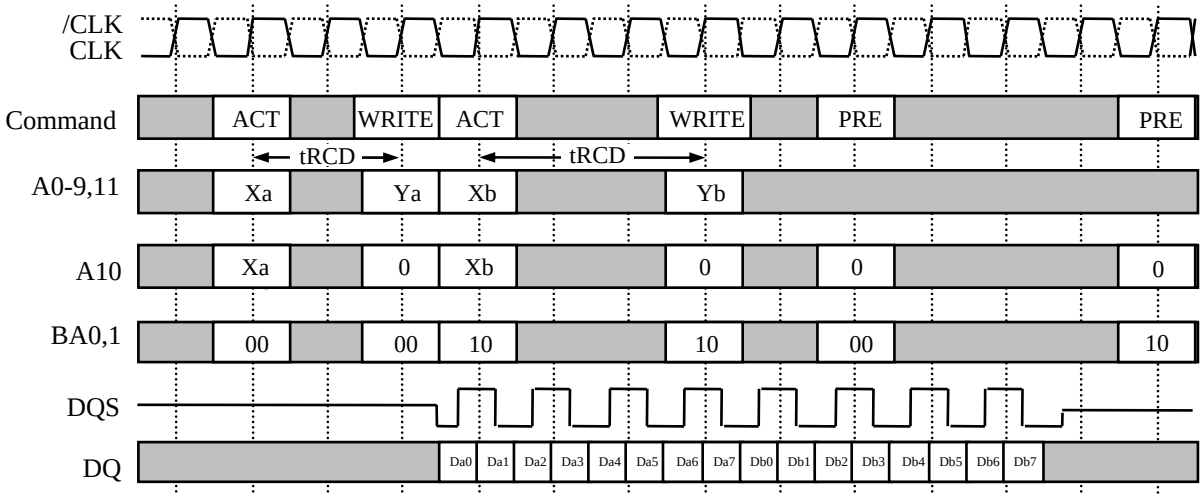
READ with Auto-Precharge (BL=8, CL=2,2.5,3.0) (tRAS determinant case)



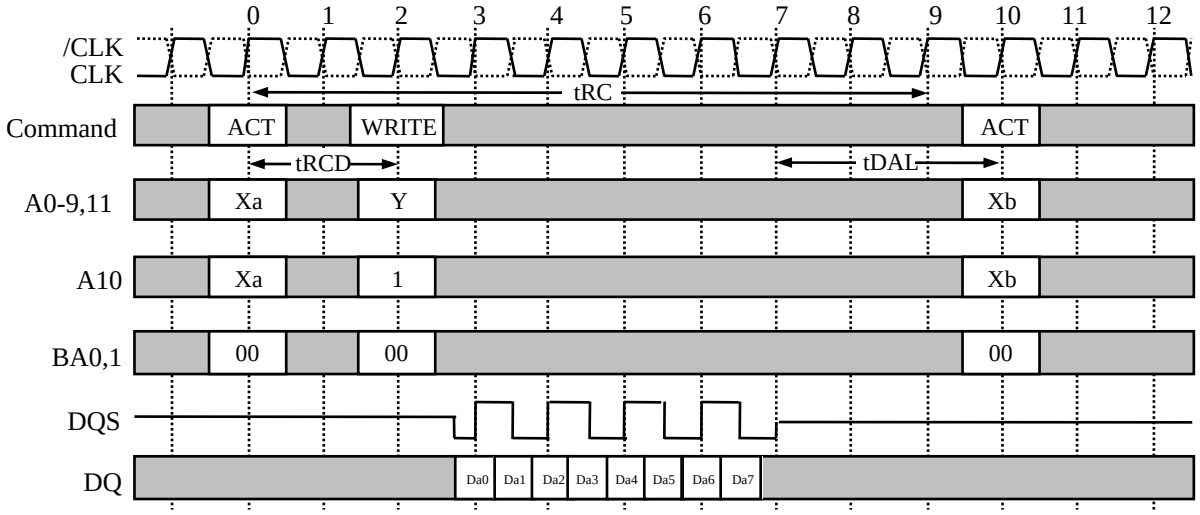
WRITE

After tRCD from the bank activation, a WRITE command can be issued. 1st input data is set from the WRITE command with data strobe input, following (BL-1) data are written into RAM, when the Burst Length is BL. The start address is specified by A0-9(x8)/A0-8(x16), and the address sequence of burst data is defined by the Burst Type. A WRITE command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous input data by interleaving the multiple banks. From the last data to the PRE command, the write recovery time (tWR) is required. When A10 is HIGH at a WRITE command, the auto-precharge(WRITEA) is performed. The next ACT command can be issued at the later time of either tDAL from the last input data cycle or tRC after ACT.

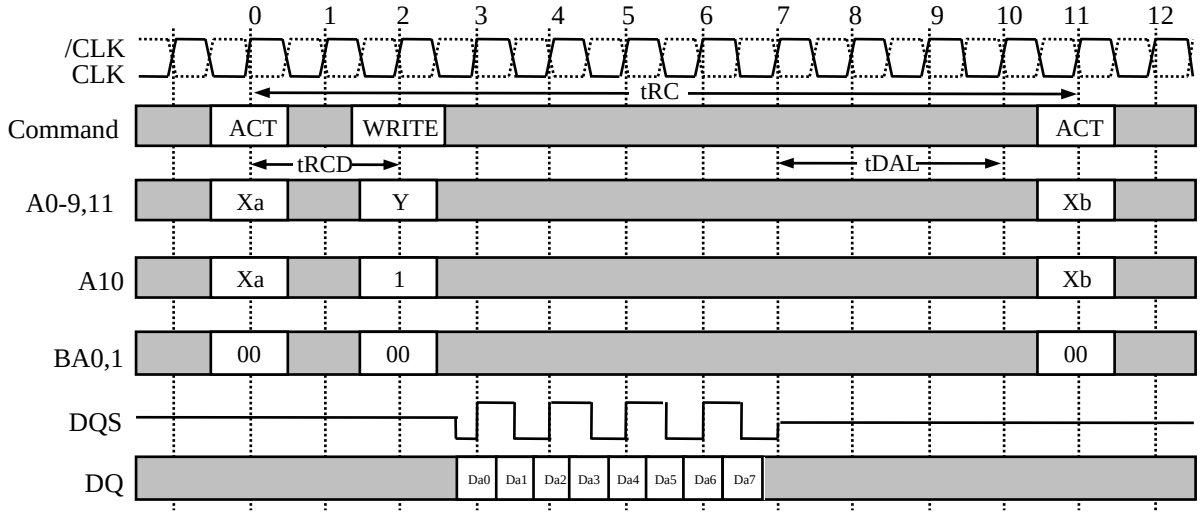
Multi Bank Interleaving WRITE (BL=8)



WRITE with Auto-Precharge (BL=8) (tDAL determinant case)



WRITE with Auto-Precharge (BL=8) (tRC determinant case)

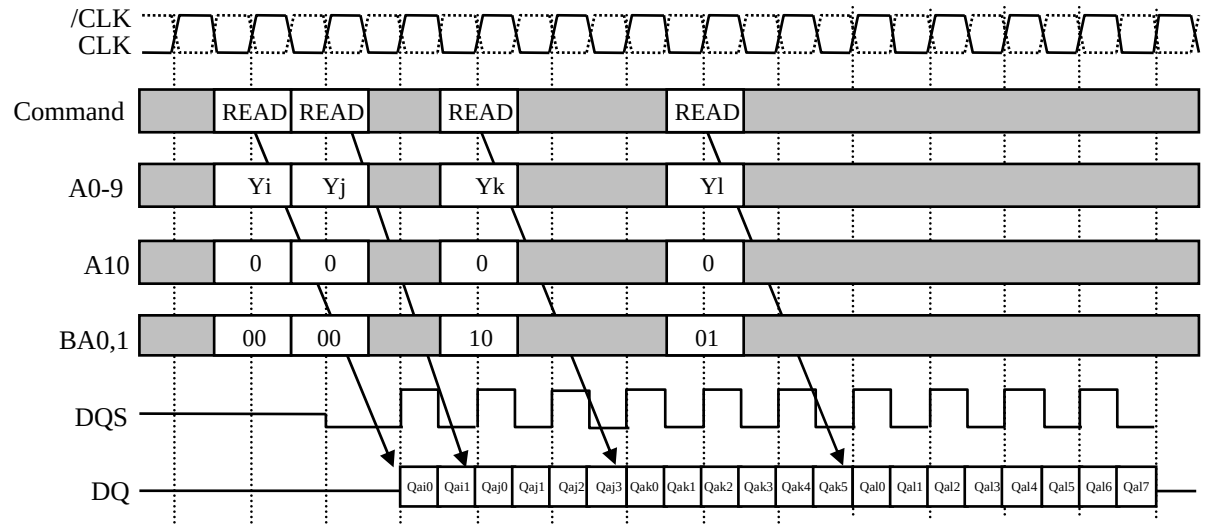


BURST INTERRUPTION

[Read Interrupted by Read]

Burst read operation can be interrupted by new read of any bank. Random column access is allowed. READ to READ interval is minimum 1CLK.

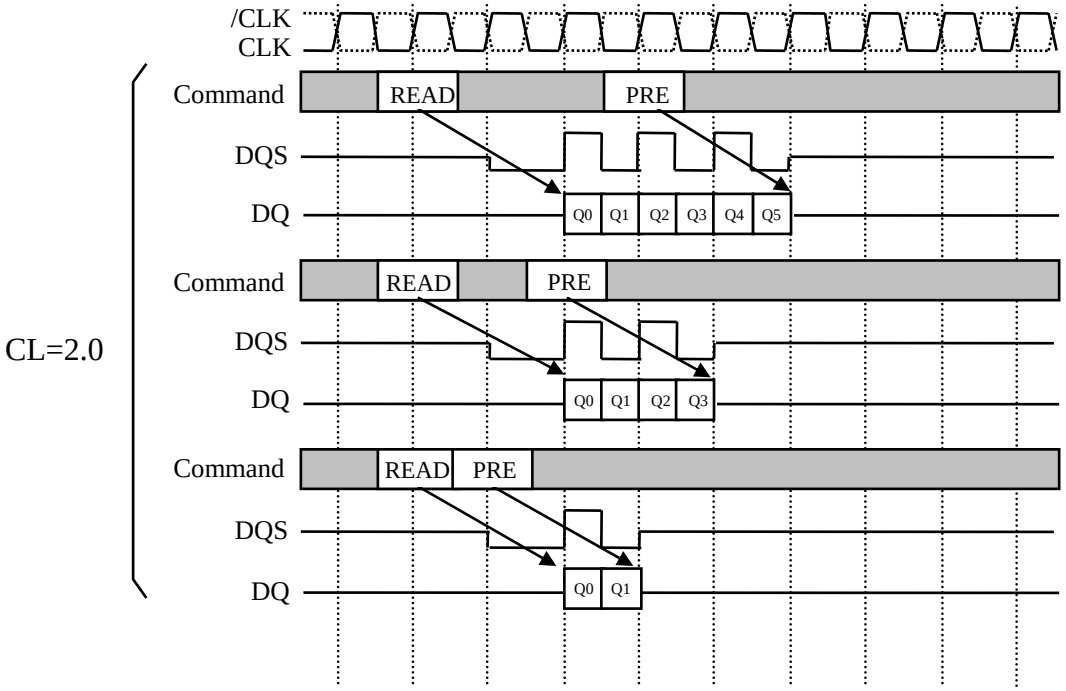
Read Interrupted by Read (BL=8, CL=2)



[Read Interrupted by precharge]

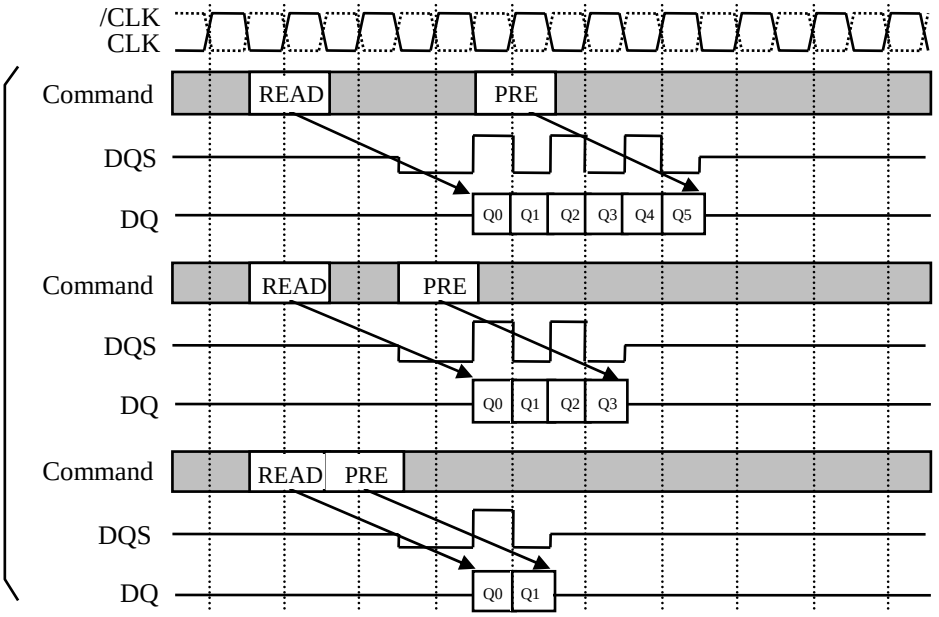
Burst read operation can be interrupted by precharge of the same bank. READ to PRE interval is minimum 1 CLK. A PRE command to output disable latency is equivalent to the /CAS Latency. As a result, READ to PRE interval determines valid data length to be output. The figure below shows examples of BL=8.

Read Interrupted by Precharge (BL=8)



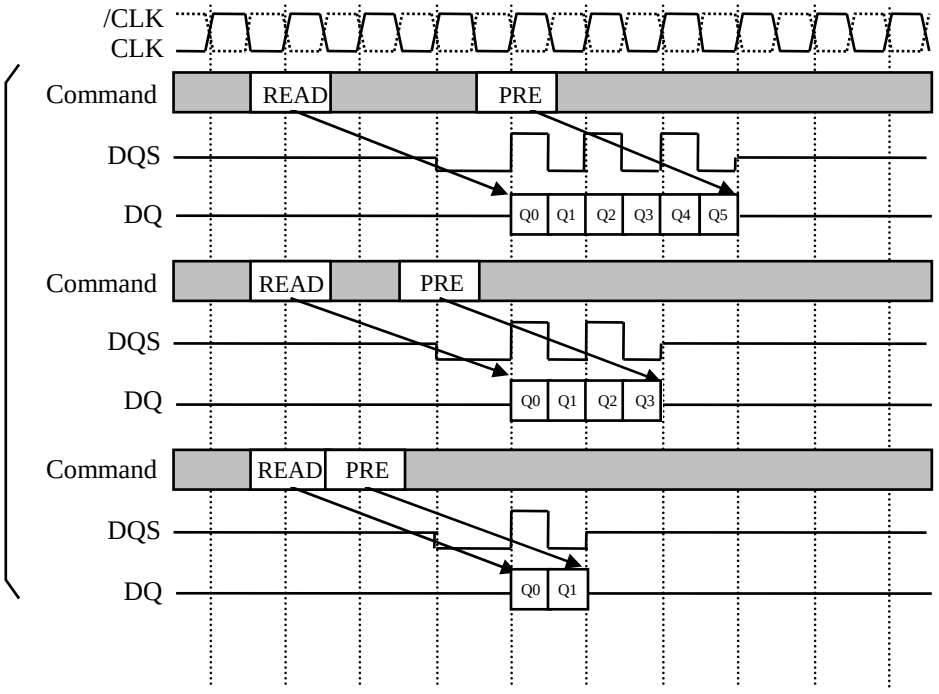
Read Interrupted by Precharge (BL=8)

CL=2.5



Read Interrupted by Precharge (BL=8)

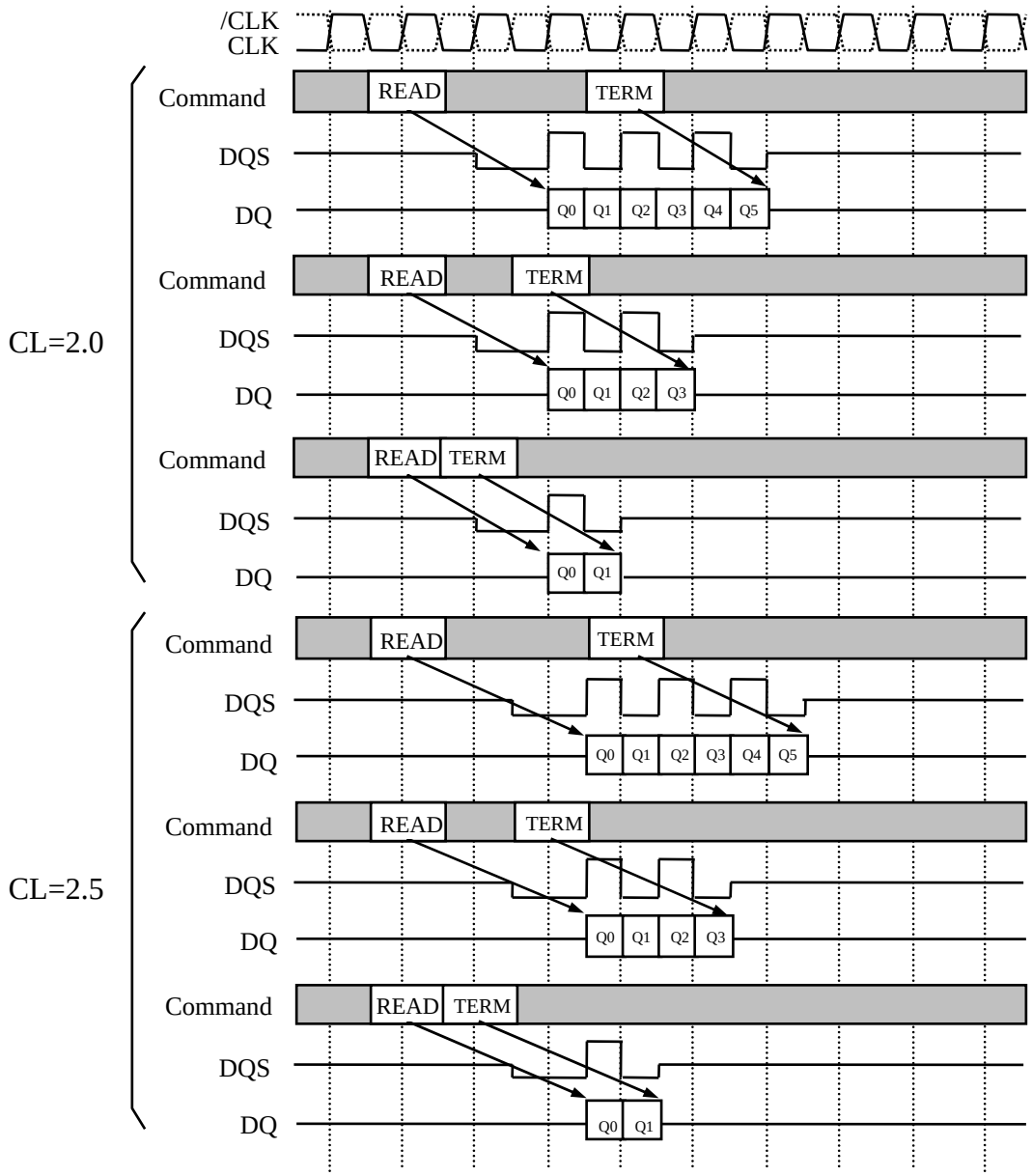
CL=3.0



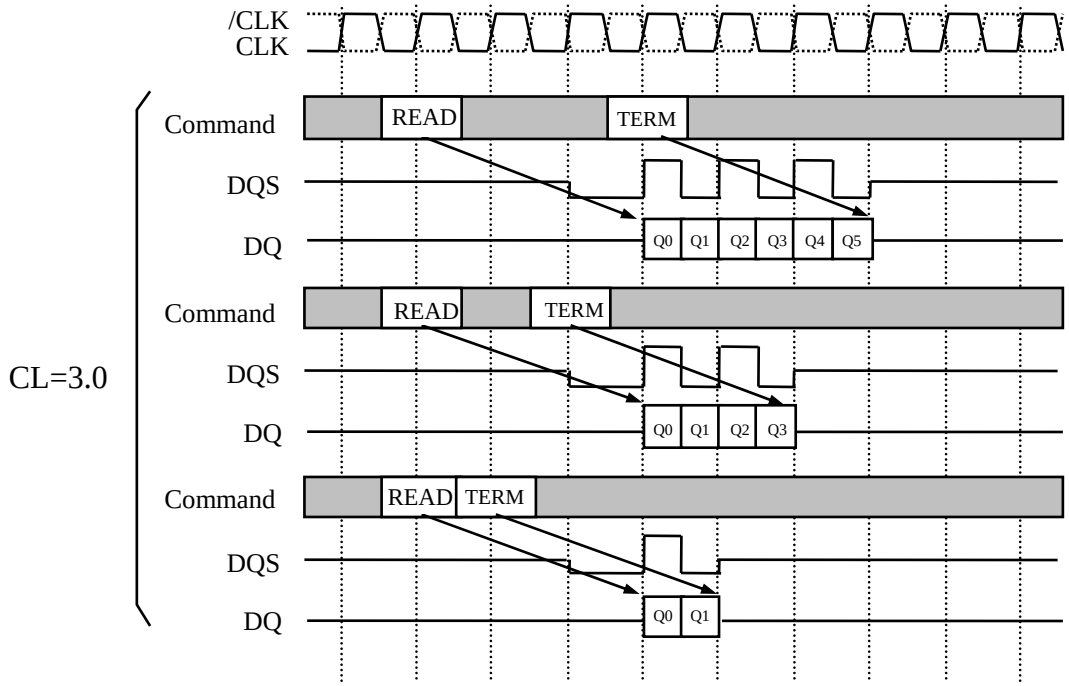
[Read Interrupted by Burst Stop]

Burst read operation can be interrupted by a burst stop command(TERM). READ to TERM interval is minimum 1 CLK. A TERM command to output disable latency is equivalent to the /CAS Latency. As a result, READ to TERM interval determines valid data length to be output. The figure below shows examples of BL=8.

Read Interrupted by TERM (BL=8)

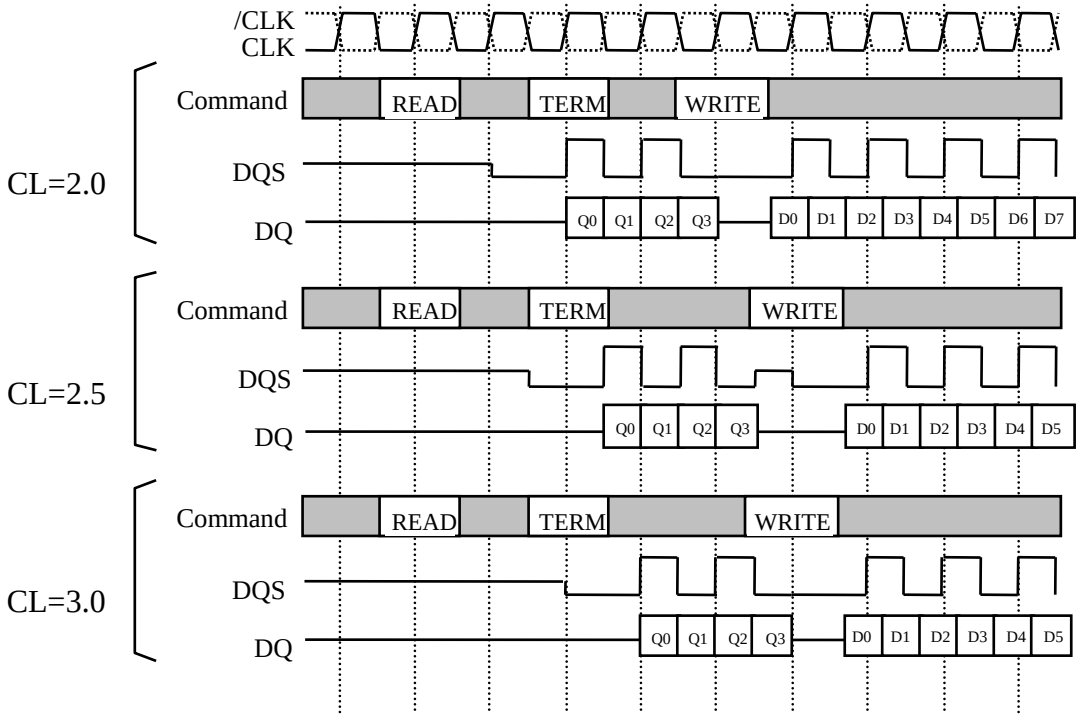


Read Interrupted by TERM (BL=8)



[Read Interrupted by Write with TERM]

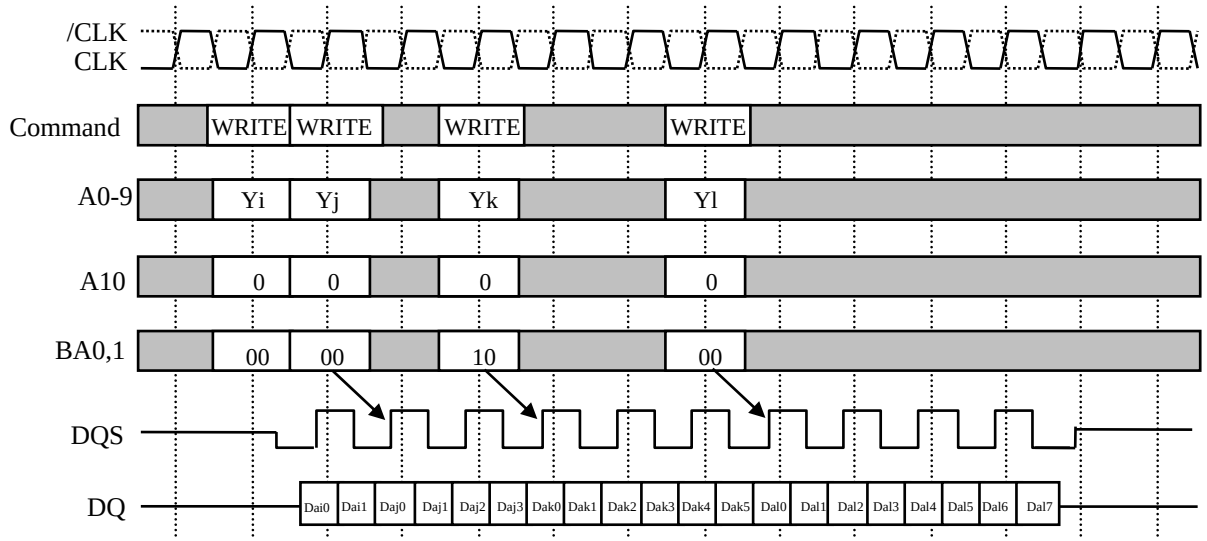
Read Interrupted by TERM (BL=8)



[Write interrupted by Write]

Burst write operation can be interrupted by write of any bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CLK.

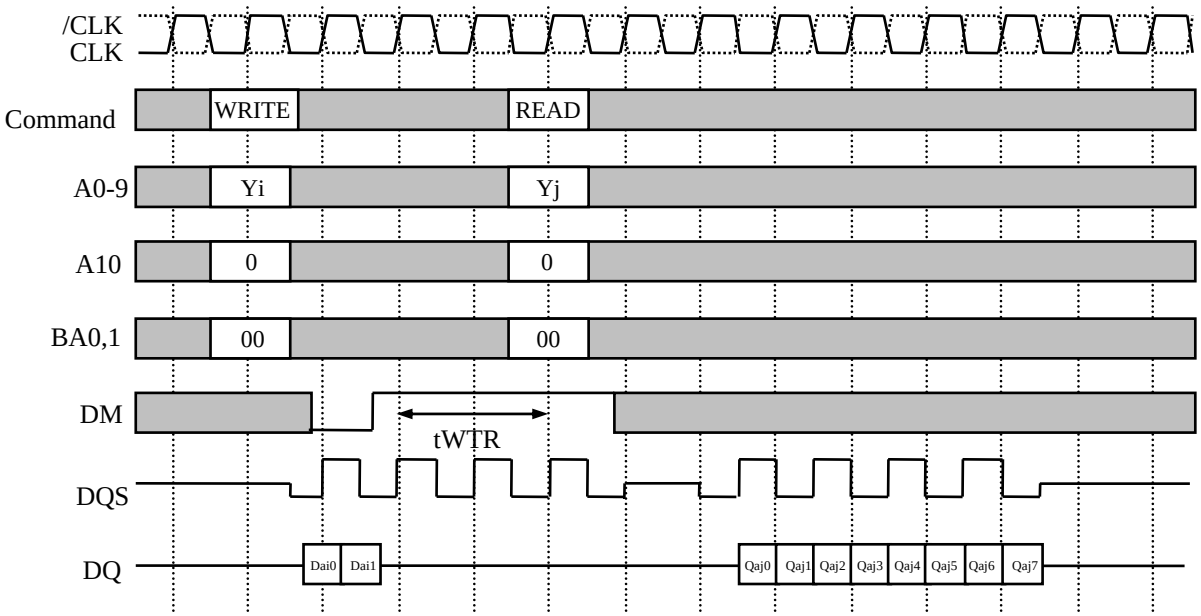
Write Interrupted by Write (BL=8)



[Write interrupted by Read]

Burst write operation can be interrupted by read of the same or the other bank. Random column access is allowed. Internal WRITE to READ command interval (tWTR) is minimum 2 CLK. tWTR is referenced from the first positive CLK edge after the last data input.

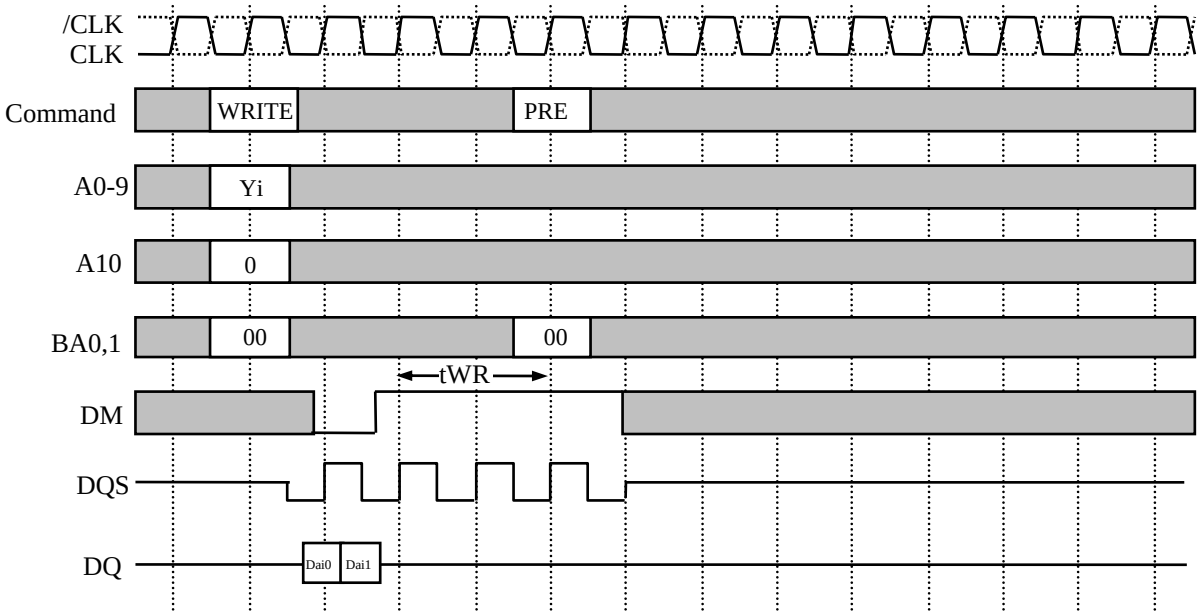
Write Interrupted by Read (BL=8, CL=2.5)



[Write interrupted by Precharge]

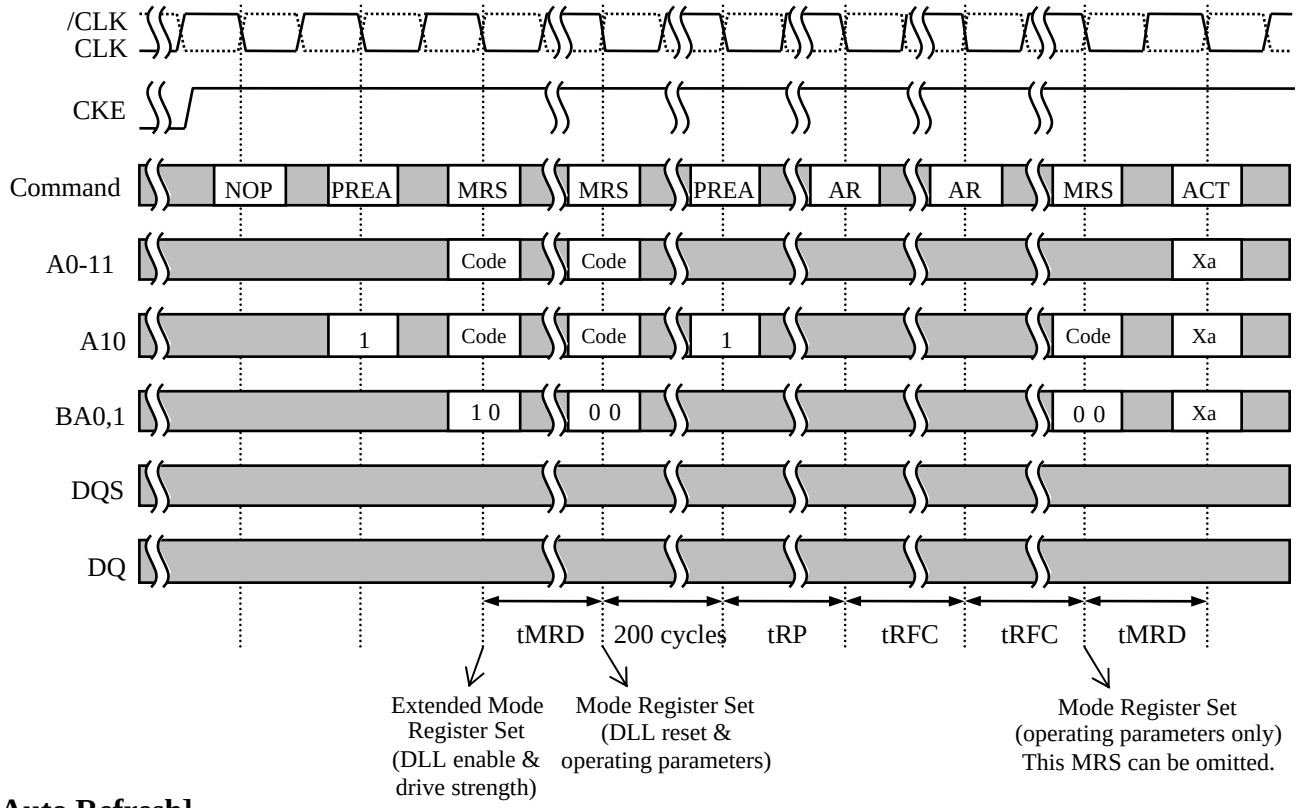
Burst write operation can be interrupted by precharge of the same or all bank. Random column access is allowed. tWR is referenced from the first positive CLK edge after the last data input.

Write Interrupted by Precharge (BL=8, CL=2.5)



[Initialize and Mode Register Sets]

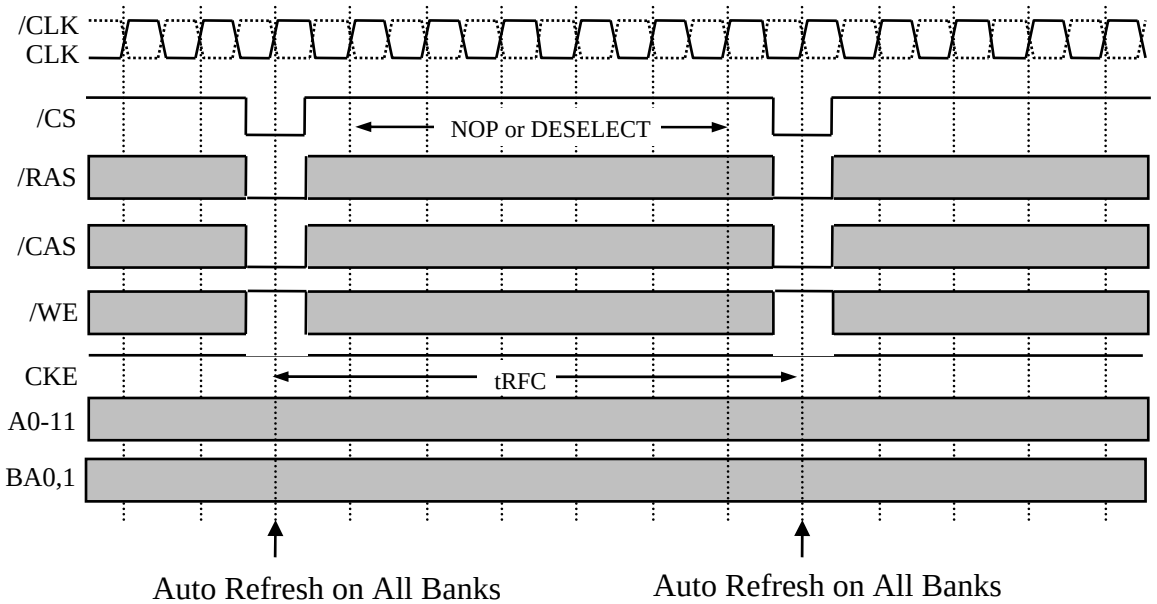
Initialize and MRS



[Auto Refresh]

Single cycle of Auto Refresh is initiated with a REFA (/CS=/RAS=/CAS=L,/WE=CKE=H) command. The refresh address is generated internally. 4096 REFA cycles within 64ms refresh 128M bits memory cells. The Auto Refresh is performed on 4 banks concurrently. Before performing an Auto Refresh, all banks must be in the idle state. Auto Refresh to Auto Refresh interval is minimum tRFC . Any executable command must not be supplied to the device before tRFC from the REFA command.

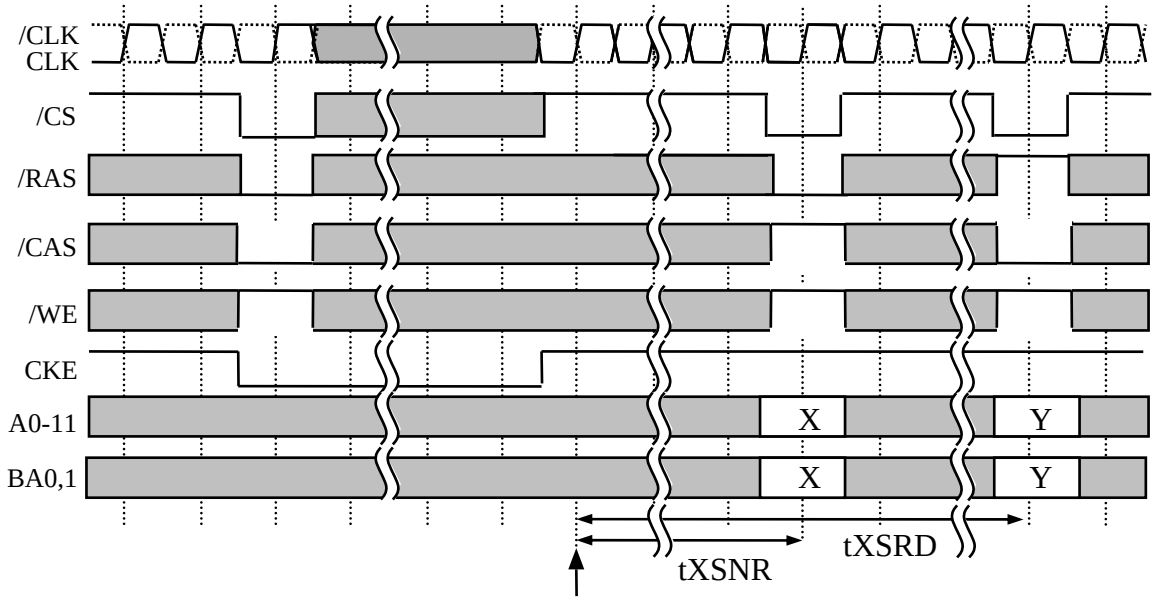
Auto Refresh



[Self Refresh]

Self Refresh mode is entered by issuing a REFS command (/CS=/RAS=/CAS=L,/WE=H,CKE=L). Once the Self Refresh is initiated, it is maintained as long as CKE is kept LOW. During the Self Refresh mode, CKE is asynchronous and the only enable input, all other inputs including CLK are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the Self Refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE for longer than tXSNR / tXSRD. The use of Self Refresh introduces the possibility that an internally timed event can be missed when CKE is raised for exit from Self Refresh. Upon exit from Self Refresh, an extra Auto Refresh command is recommended.

Self Refresh

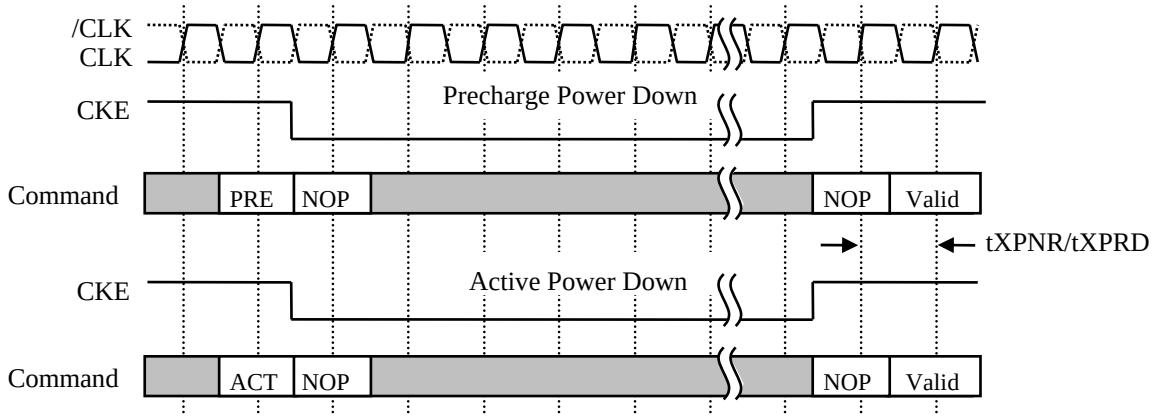


Self Refresh Exit

[Power Down]

Power Down is entered when CKE is registered LOW (no accesses can be in progress). If Power Down occurs when all banks are idle, this mode is referred to as Precharge Power Down; if Power Down occurs when there is a row active in any bank, this mode is referred to as Active Power Down. During Power Down mode, all input and output buffers excluding CLK, /CLK, and CKE are deactivated. Power Down mode is synchronously exited by registering CKE HIGH (along with a NOP or DESEL command).

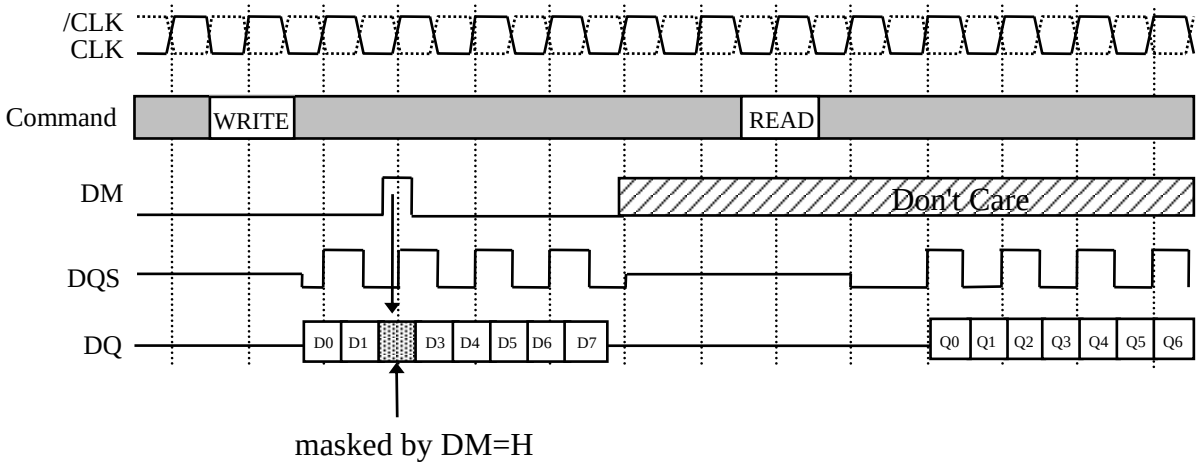
Power Down by CKE



[DM Function]

DM is defined as the data mask for writes. During writes, DM masks input data word by word. DM to write mask latency is 0.

DM Function(BL=8,CL=2)



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